University of Innsbruck

Faculty of Mathematics, Computer Science and Physics

Institute of Experimental Physics

Master Thesis

Fabrication and Characterization of Superconducting Microwave Resonators featuring new Vacuum-Gap Structures

by

Christian Schlager

April 11, 2022

Supervised by **Univ.-Prof. Dr. Gerhard Kirchmair**

Abstract

The development of low-noise amplifiers in the last 15 years was key for the recent boom in quantum information science. However, broadband amplifiers have yet to reach the quantum limit. Currently, traveling wave parametric amplifiers (TWPAs) are the leading competitor for this task. The non-linear transmission lines enabling amplification in TWPAs possess an intrinsically high inductance per unit length, which has to be addressed either by impedance transformation or by additional capacitance. In this thesis, we develop a fabrication process for tunnel-like vacuum-gap microstrip transmission lines. The multi-step fabrication process relies on a layer of sacrificial resist as a place holder for the vacuum gaps separating a central conductor from the tunnel-like ground plane above it. The sacrificial resist is then removed through holes in the ground plane via plasma etching. The resulting tunnel-like structures promise high capacitance per unit length because of the small separation between the central conductor and ground plane while avoiding excessive dielectric loss by having the dielectric removed from that gap.

To assess the microwave performance of the transmission lines created with this method, resonators in two different designs, one in complete vacuum-gap microstrip and one in a CPW design with air-bridges, are fabricated. These samples are measured in a dilution refrigerator. We report a low-power internal quality factor of 1000 for the vacuum-gap microstrip and 20 000 for the bridged CPW resonators. This places our newly developed design well within what is achieved by conventional microstrip designs used in TWPAs. Given also the potential for improvement on various aspects, this result is an excellent starting point for the development and construction of a vacuum-gap microstrip TWPA.

Acknowledgements

I would like to express my gratitude towards my supervisor Prof. Dr. Gerhard Kirchmair for giving me the opportunity of this master thesis and also thank him as well as the rest of the research group for their help and advice. Among all colleagues, special thanks have to go to Romain Albert for his kind guidance and highly appreciated support during the whole project. I am also grateful to Prof. Dr. Martin Beyer and Simone Schirra for enabling the AFM measurement, which forms a valuable part of this thesis. Finally, I want to thank my family and friends for their encouragement and loving support.

Contents

Chapter 1

Introduction

Thanks to decades of intensive research since the first conceptual ideas [1], quantum computers are well on their way to becoming reality [2]. This becomes apparent in the rapid development on multiple fronts and platforms, from the demonstration of quantum supremacy with a superconducting qubit chip [3] over promising new on-chip realizations of trapped-ion quantum computer architectures [4] to the developments in quantum error correction [5] and quantum algorithms [6].

In the ongoing research effort, superconducting qubits are one of the most prominent platforms for the development of quantum computers [7, 8]. The most distinctive advantages this approach offers are, the possibility to design qubits and not have to rely on naturally occurring systems like ions and the scalability potential promised by on-chip fabrication. Additionally, the superconductivity of the used components offers high coherence times compared to typical gate speeds.

When realizing dispersive non-demolition readout of qubits, the signals carrying the extracted information consist only of a few photons at microwave frequencies. This means amplification near the quantum limit is essential for single-shot measurements. Quantum-limited [9] amplifiers are therefore an important building block for modern quantum science [10].

The first devices approaching the quantum limit were resonant parametric amplifiers [11–15]. Because of their resonant design, the amplification bandwidth is limited to a few tens of MHz, depending also on the gain that should be achieved [16]. In the last few years, the prospect of overcoming this limitation has brought a lot of attention on a special form of the parametric amplifier. Due to its non-resonant geometry, the traveling wave parametric amplifier (TWPA) is able to exceed the bandwidths of resonant parametric amplifiers by orders of magnitude, opening up many new applications [17]. By enabling frequency multiplexing for multi-qubit architectures or arrays of superconducting detectors [18], TWPAs will be a game-changer for the fields of quantum research, quantum computing, and astronomy. TWPAs have already been successfully implemented in a variety of different designs [19–34], but are still limited by a number of issues, as will be discussed
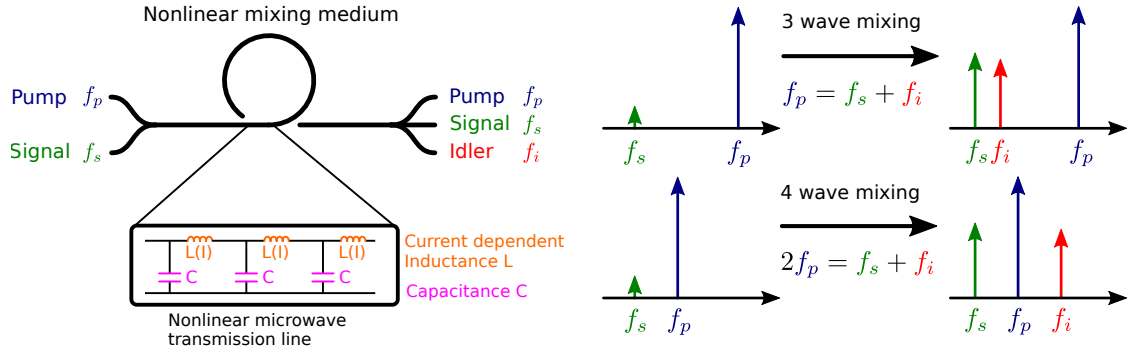
Figure 1.1: Schematic of parametric mixing in a nonlinear medium. For microwaves, the nonlinearity is realized by a transmission line with current dependent inductance. By interaction through the nonlinear medium, pump photons are converted to signal and idler photons providing amplification of the signal. Depending on the order of the nonlinearity and the mode of operation this conversion happens as a three-wave mixing or four-wave mixing process.

more thoroughly in chapter 2 and section 3.3.3.

The fundamental working principle of a TWPA relies on the nonlinearity of the propagation medium, analogous to an optical parametric amplifier (OPA) [35, 36]. The nonlinearity of the medium allows for the conversion of photons of a strong pump tone to signal and idler photons through a process similar to stimulated emission. This interaction can occur as three-wave mixing (3WM) or four-wave mixing (4WM). Depending on the order of the mixing process one (for 3WM) or two (for 4WM) pump photons are destroyed to create a pair of signal and idler photons. Figure 1.1 shows this principle and also the implementation of a nonlinear medium for microwave frequencies. The nonlinearity of the transmission line serving as the mixing medium is provided by the dependence of the inductance on the current through the line. This can be achieved either by using the intrinsic nonlinear inductance of Josephson junctions (JJs) [37, 38] or by choosing a high kinetic inductance material (see section 3.2.2) for the transmission line.

As the origin of the nonlinearity is the inductance, TWPA transmission lines have a significantly increased inductance. This gives rise to the problem of matching the impedance of the nonlinear transmission line of a TWPA to the usual $50\,\Omega$ (see chapter 2). Therefore, in this thesis, we will present a newly developed fabrication process, capable of producing high-capacitance vacuum-gap transmission lines. The increased capacitance of these lines can be used to compensate for the increased inductance.

This thesis is divided into 7 chapters. Chapter 2 starts with explaining the context of our newly developed fabrication process, why it is useful, and how it can possibly be used to improve the performance of TWPAs. In chapter 3 the theoretical basics of microwave technology, kinetic inductance, and quantum-limited amplification are explained. Chapter 4 introduces a selection of fabrication methods before going through the newly developed fabrication process for vacuum-gap microstrips. It finishes by highlighting a number of challenges encountered during the development

of the process along with the ideas and methods that were used to overcome them. In chapter 6 we first present a thorough examination of the fabricated structures using scanning-electron and atomic-force microscopy. Then the results of the measurements that were done on the fabricated samples in a cryogenic environment are analyzed and discussed. The thesis is completed by a conclusion of the findings and an outlook on possible next steps and newly opened possibilities. Finally, in the appendix, the reader can find the fabrication recipe in a more compact form.

Chapter 2

The TWPA Capacitance Challenge

The apparent advantages of TWPAs in terms of their bandwidth are also accompanied by a number of challenges that have to be faced. The implementation as a transmission line instead of a resonator calls for longer devices to achieve comparable amplification to resonant parametric amplifiers. Also phase matching of the involved microwave tones becomes a concern (see 3.3.3).

In this chapter, we will deal with another problem resulting from the transmission line geometry of TWPAs. We will motivate why traveling wave parametric amplifiers call for high capacitance transmission lines, show different approaches in realizing them, and also talk about specific problems arising with each solution. Then the vacuum-gap microstrip, that was developed in this thesis, will be introduced as a way to achieve high capacitance in a transmission line while keeping the losses as low as possible. Finally we discuss approaches similar to ours, that have already been made by previous research.

2.1 Transmission Line Impedance Matching

To maximize the efficiency of traveling-wave parametric mixing processes and to keep the length of the amplifying devices reasonable, the nonlinear inductance should be large compared to the geometric inductance of the transmission line. The fabrication of nonlinear transmission lines using high kinetic inductance materials or metamaterials is the target of intensive research [39, 40]. However, the large additional inductance of those transmission lines leads to increased characteristic impedance ($Z = \sqrt{L/C}$). If no countermeasures are taken, the increased impedance causes unwanted reflections at the ends of the transmission line and thereby deteriorates the performance of the amplifiers.

The first way to go about the higher characteristic impedance is to try to mitigate impedance mismatch effects using impedance transformers [19–22]. However, this is hard to do over the large bandwidths of TWPAs. The remaining reflections at the transformers often lead to ripples in the

gain spectrum of the TWPAs, effectively limiting the gain that can be achieved [22]. Large gain, however, is necessary to overcome the noise introduced by later amplification stages and other components in the measurement setup. Another way is to counteract the large inductance and match the device to the usual $50\,\Omega$ of characteristic impedance by increasing the capacitance per unit length.

Capacitance is required for many nano-electronic and nano-electric applications. If capacitances are to be integrated on-chip, the usual way to do so is either by coplanar design or by implementing a parallel-plate capacitor in a multi-layer process, deploying a dielectric layer in between two metal plates. The same principles are applied in superconducting circuits used in circuit quantum electrodynamics (cQED).

To increase the capacitance per unit length of the nonlinear transmission lines of TWPAs, different approaches have been taken.

- The first attempts to increase the capacitance per unit length were to include lumped-element capacitors [23–26], deploying dielectric thin-films. In contrast to the crystalline substrate of a wafer, the amorphous structure of thin-film dielectrics leads to generally higher losses. For many circuit QED applications, also including TWPAs, low losses are essential. While resistance vanishes for superconductors, other sources of loss become dominant and in fact dielectric losses are often the limiting factor for the noise performance of TWPAs [17].

- Implementing the TWPA in a classic microstrip geometry (see section 3.1.1) also increases capacitance [27–31]. The base conductors are covered by a dielectric (Al_2O_3 for [28, 29], amorphous Si for [27, 30, 31]), on which a ground plane is deposited. The capacitance of all structures is greatly enhanced by the close ground plane, separated from the central conductor only by the dielectric film thickness, typically a few tens of nanometers. However, as for the lumped-element capacitors, the problem of high losses in amorphous thin-film dielectrics remains.

- A method to avoid lossy dielectrics while still obtaining large capacitance is to implement distributed interdigitated capacitors [32–34]. The large capacitance in those is not obtained by close distance, like in the examples before, but by large area. By implementing structures in an interdigitated geometry, as shown in fig. 2.1, sufficient capacitance can be obtained despite the typical separations in the order of µm between the conducting track and the ground plane. In contrast to the approaches using dielectric thin films, the electric fields in this design are located either in the free space above the wafer or within the crystalline dielectric (see section 3.1.1), leading to comparably low losses. Problems associated with interdigitated capacitor designs are the possible appearance of parasitic resonances as well as increased sensitivity to fabrication defects because of the large footprint.

To conclude, every approach offers advantages but also has its drawbacks, which ultimately limit
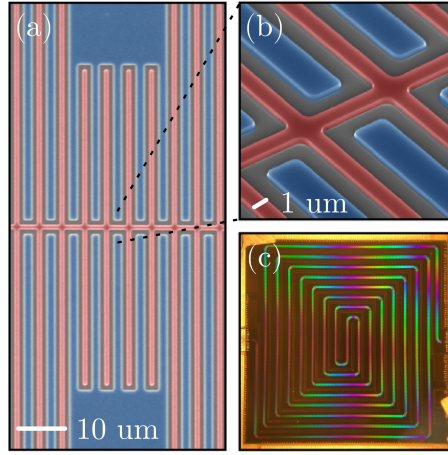
Figure 2.1: Implementation of a TWPA with interdigitated capacitors along the transmission line in the work of Malnou et al. [32]. **(a)** and **(b)** Transmission line (false color red) is loaded with interdigitated capacitors that generate capacitance between the line and the ground plane. Also they are used for phase matching by dispersion engineering. **(c)** The complete TWPA with a length of 33 cm fits on a 2 cm by 2 cm chip in a spiral configuration.

the performance of TWPAs. The fabrication process developed in this thesis promises to achieve the convenient and compact high capacitance of the microstrip approach with low dielectric loss. We developed a method for creating vacuum-gap microstrips with high capacitance thanks to the small ($<100\,$nm) separation between central conductor and ground plane and low dielectric loss. The fabrication and characterization of such vacuum-gap microstrips is the heart of this thesis.

2.2 Vacuum-Gap Microstrips

To combat the problem of excessive dielectric loss in the microstrip design we developed a fabrication process for a vacuum-gap microstrip, a design that replaces the dielectric layer of a microstrip with a vacuum gap. The reasoning behind this is of course that the most direct way to prevent dielectric losses is by removing the dielectric. The vacuum-gap microstrip lines are realized as free-standing tunnels over a central conductor as illustrated in fig. 2.2. Here microstrip refers to the geometry of the transmission line. Details on different geometries of transmission lines will be given in section 3.1.1. To maximize capacitance, the height of the tunnel is kept as low as easily feasible with a resist as a place holder. With that distance being in the range of 100 nm, it is clearly in the regime, where the ground plane on top, i.e. the roof of the tunnel is much closer to the central conductor than the sidewalls of the tunnel, which are a few µm away. Further information on the actual dimensions of the sample and the realization of the tunnels is given in sections 4 and 5.

In addition to the application as a high capacitance transmission line, such supported tunnel structures are suited for a second application. Patterned into more narrow bridges instead of extended tunnels they form air-bridges. Those can be used for ground plane connection where it is separated for example by CPW lines. This prevents slot line modes, that otherwise have to be counteracted by either on-chip wire bonds [34, 41] or other elaborate sample or sample holder designs [32].
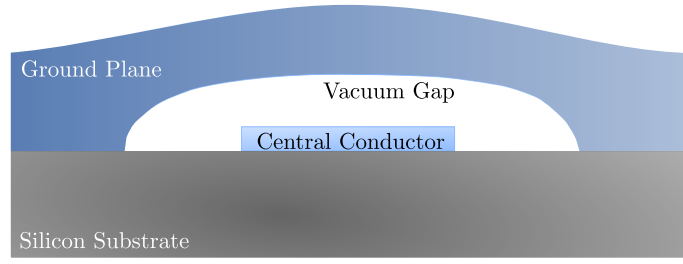
Figure 2.2: Schematic of the vacuum-gap microstrip. The idea is to fabricate a transmission line in a narrow gap microstrip design and to remove the dielectric afterward. The ground plane is forming a free-standing tunnel above the central conductor and is separated from it by a thin vacuum gap.

To conclude, we want to use supported tunnel-like structures to obtain large capacitance on the whole length of a transmission line, while avoiding excessive loss caused by a dielectric thin film. With that design, it is possible to compensate for a high-inductance central conductor and keep the characteristic impedance at the conventional $50\,\Omega$. This makes our developed fabrication process for a vacuum-gap microstrip transmission line a promising starting point for the construction of a quantum-limited TWPA.

2.3 Existing Microstrip and Air-Bridge Designs

The idea of using supported structures to obtain high capacitance or to build air-bridges for improved ground plane connection is not new. In a 2D environment like a wafer, the necessity often arises to bridge appearing gaps by using the third dimension. Especially the need to avoid slot line modes in CPW geometries has made air-bridges an important resource of micro- and nano-fabrication [42, 43].

To realize high capacitance for the use in resonators, lumped-element vacuum-gap capacitors have already been implemented using a similar principle to what we will describe in this thesis [44, 45]. Similar to our process, a sacrificial layer separates the two electrodes of a large parallel-plate capacitor during fabrication and is removed afterward. In these works, however, the sacrificial layer is made from materials (Al in [44], Nb, Si or SiN_x in [45]), the removal of which introduces chemical incompatibilities with commonly used superconducting materials. The fabrication process described in this work uses a resist, that can be removed by oxygen plasma etching, which preserves the compatibility with both, aluminum and niobium as possible components for the base layer. Moreover, to our knowledge, a similar design was not yet implemented as a transmission line.

For the use in a TWPA, especially the losses of devices fabricated using our newly developed fabrication process are relevant. Comparing it to the work of others that have already utilized microstrip designs for the realization of TWPAs is interesting for assessing the potential offered by our approach. As figure of merit we use the loss tangent $\tan\delta = \frac{1}{Q_i}$ (see section 3.1.3). The numbers given in table 2.1 are taken from works on TWPAs using a microstrip geometry to obtain sufficient capacitance or from preceding papers specifically treating the used transmission lines. One has to

Table 2.1: Implementations of TWPAs using the microstrip design have encountered limitations because of their dielectrics. The relevant figure of merit for the performance of a dielectric is the loss tangent $\tan\delta = \frac{1}{Q_i}$.

publication	dielectric	loss tangent $\tan\delta$
Shan et al. [27],[46]	50 nm SiO$_2$	5×10^{-4}
Ranadive et al. [29],[40]	30 nm Al$_2$O$_3$	4×10^{-3} to 6.5×10^{-3}
Planat et al. [28],[40]	28 nm Al$_2$O$_3$	6.5×10^{-3}
Shu et al [31]	200 nm aSi:H	3.6×10^{-5}

consider, that it is difficult to classify the origin of the losses, and also the loss properties of the TWPAs are not guaranteed to be the same as for the test devices. However, the numbers give a good impression of the state of the art of nonlinear, high capacitance transmission lines and their limits.

The loss tangents achieved with thin-film dielectric microstrips in TWPAs so far, are in the range from approximately 5×10^{-4} to 5×10^{-3}, resulting in quality factors of 200 to 2000. The only exception we know of is the TWPA demonstration from Shu et al. from 2021. With a loss tangent of $\tan\delta = 3.6 \times 10^{-5}$ or a quality factor of $Q_i = 2.8 \times 10^4$ it shows significantly less loss than previous works.

To summarize, one can say, that the impedance matching of nonlinear transmission lines for use in TWPAs remains challenging. The large inductance needed for an efficient mixing process calls for additional capacitance to keep the characteristic impedance at the usual $50\,\Omega$. The thin-film dielectrics often used to achieve large capacitance introduce additional noise in TWPAs because of their loss. This issue has been addressed with different approaches but is still far from being completely resolved.

2.4 Potential

A simple estimate of the losses that can be expected from the vacuum-gap microstrip can be used to demonstrate its potential. The low-power losses of a superconducting resonator without an amorphous dielectric are dominated by two-level systems (TLS) on surfaces and interfaces [47]. The numbers reported for the loss tangent of aluminum oxide, which we expect to cover the metal-to-vacuum interfaces in our design range from 10^{-4} to 2×10^{-3} [48] for different deposition methods. Specifically for plasma oxidation Deng et al. report $\tan\delta = 1.5 \times 10^{-3}$ to 2×10^{-3} [49]. The surface of the silicon substrate could also be relevant, as it might contain lossy amorphous oxides as a result of the fabrication process. The loss tangents found for those range from $\tan\delta = 10^{-3}$ to 10^{-2} [48]. Compared to these lossy dielectrics the loss tangent of the bulk silicon with $\tan\delta < 10^{-7}$ [50] can be neglected.

Without detailed analysis of the final surfaces and simulations of the electric field distribution, it is difficult to estimate the participation ratios of the different dielectrics for our vacuum-gap microstrip design. Based on the geometry, with a gap height of approximately 100 nm and an assumed oxide

layer thickness of a few nm, we anticipate the aluminum oxide to have a participation ratio in the range of $1\,\%$ to $10\,\%$ and to dominate over the silicon oxides. This results in an effective loss tangent in the range of 10^{-4} to 10^{-5} that should be achievable in a best-case scenario. In terms of quality factor this corresponds to 10^4 to 10^5. Comparison with the losses of transmission lines used in previous successful TWPA implementations (see table 2.1) the potential offered by the vacuum-gap approach is evident.

Chapter 3

Basic Concepts and Theory

In this chapter, we will provide a few basic concepts necessary for later discussions and also introduce the theoretical background used in our analysis. The first part of the chapter is treating basic microwave theory, notably microwave transmission lines and resonators, and how to quantify their performance. The second part focuses on introducing superconductivity and the central concept of kinetic inductance. The final part of this chapter is dedicated to quantum-limited amplifiers, their working principle and the distinction between resonant parametric amplifiers and TWPAs.

3.1 Microwave Technology Basics

For further understanding of the concepts presented in this thesis, it is necessary to introduce a few ideas and calculations of microwave engineering theory. For a more rigorous and complete treatment of the topic, the reader is referred to [51].

3.1.1 Transmission Lines

Transmission lines are a fundamental component of microwave technology. They enable the propagation of signals between components and can, in the case of nonlinear transmission lines, be used as an active component in the circuit.

Telegrapher's Equation

To understand electromagnetic waves in a transmission line, it is useful to start with a lumped-element model. We consider TEM waveguides that can be modeled by a series of lumped-element unit cells. As shown in fig. 3.1 we need four different elements to account for the lines resistance R, inductance L, capacitance C between the conductors and finally dielectric losses which is accounted for with a shunt resistance G. This unit cell is repeated in z-direction to form the transmission line. R, L, C, and G are the respective values per unit length and therefore each have to be multiplied by the length Δz of our short unit cell to give the value for the lumped-element circuit. The figure
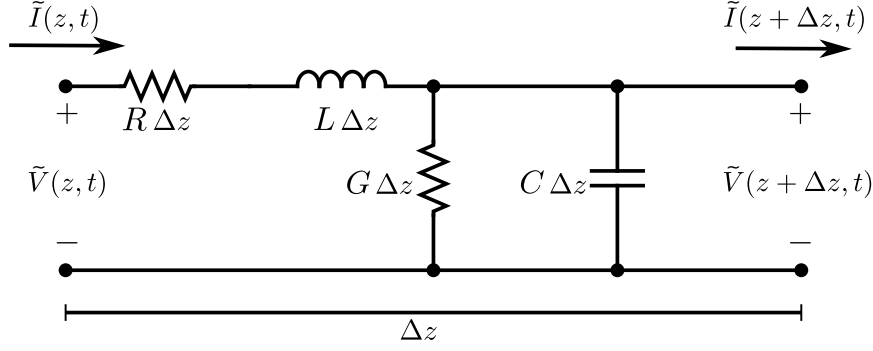
Figure 3.1: Lumped-element model of a transmission line. Image similar to [51]. For the lossless model one assumes $G = R = 0$.

also defines the current $\tilde{I}(z,t)$ and voltage $\tilde{V}(z,t)$ for the location z along the line and at the time t. Applying Kirchhoff's current and voltage law to the circuit in fig. 3.1 and taking the limit of $\Delta z \to 0$ one obtains the *telegrapher equations*

$$\frac{\partial \tilde{V}(z,t)}{\partial z} = -Ri(z) - L\frac{\partial \tilde{I}(z,t)}{\partial t} \tag{3.1.1}$$

$$\frac{\partial \tilde{I}(z,t)}{\partial z} = -Gv(z) - C\frac{\partial \tilde{V}(z,t)}{\partial t}. \tag{3.1.2}$$

Assuming sinusoidal time evolution of current and voltage ($\tilde{V}(z,t) = V(z)e^{i\omega t}$, $\tilde{I}(z,t) = I(z)e^{i\omega t}$) these equations are reduced to

$$\frac{dV}{dz} = -(R + i\omega L)I(z), \tag{3.1.3}$$

$$\frac{dI}{dz} = -(G + i\omega C)V(z). \tag{3.1.4}$$

From solving the wave equations that follow after differentiating and inserting equations (3.1.3) and (3.1.4) into one another one obtains the traveling wave solutions for voltage and current,

$$V(z) = V^+ e^{-\gamma z} + V^- e^{\gamma z} \tag{3.1.5}$$

$$I(z) = I^+ e^{-\gamma z} + I^- e^{\gamma z} \tag{3.1.6}$$

that include waves traveling in the positive and negative z-direction. The complex propagation constant γ is given by

$$\gamma = \alpha + i\beta = \sqrt{(R + i\omega L) \cdot (G + i\omega C)}. \tag{3.1.7}$$

In the limit of a lossless line ($R = G = 0$), some relevant parameters of the transmission line simplify. These are the propagation constant

$$\gamma = i\beta = i\omega\sqrt{LC}, \tag{3.1.8}$$

the wavelength

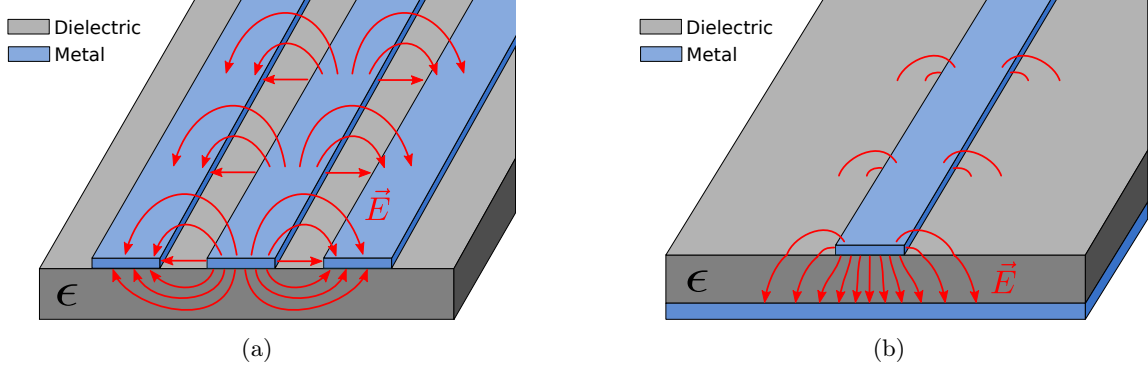$$\lambda = \frac{2\pi}{\beta}, \tag{3.1.9}$$

Figure 3.2: The two planar transmission line designs relevant for this thesis are the coplanar waveguide (CPW) and the microstrip. Both designs feature a dielectric (gray), characterized by its electric permittivity ϵ and metal stripes (blue). The electric field distribution is indicated with red arrows. **(a)** Coplanar waveguide. Gaps on each side separate the central conductor from the return conductors. **(b)** Microstrip. The conducting track and the ground plane are separated by a dielectric.

and the phase velocity

$$v_{ph} = \frac{1}{\sqrt{LC}} \tag{3.1.10}$$

For later discussions, it is important to understand the meaning and properties of the characteristic impedance Z. By definition it is given by the ratio between voltage and current of a forward traveling wave in the transmission line

$$Z := \frac{V^+}{I^+} = \sqrt{\frac{L}{C}}. \tag{3.1.11}$$

For a transmission line with impedance Z_0 terminated with a load with impedance Z_L, a mismatch in impedance results in the generation of reflected waves. One can show that the voltage amplitude V^- of the reflected wave is related to the voltage amplitude V^+ of the incident wave via

$$V^- = V^+ \cdot \frac{Z_L - Z_0}{Z_L + Z_0} = \Gamma V^+, \tag{3.1.12}$$

where Γ is referred to as the reflection coefficient. In terms of average power delivered to the load we get

$$P_{avg} = \frac{|V^+|^2}{2Z_0}(1 - |\Gamma|^2). \tag{3.1.13}$$

Designs

Different designs are used for realizing planar microwave transmission lines. Because of their relevance in this thesis, we will focus on two of them, namely the microstrip and the coplanar waveguide (CPW). The two designs are represented in fig. 3.2.

A coplanar waveguide consists of a central conductor accompanied by a return conductor on each side (in the same plane, therefore the name). The electric field is partly in the dielectric substrate and partly in the space above it. The participation ratio of the dielectric, meaning the fraction of electric field energy that is stored in it depends on the specific dimensions and the electric permittivity ϵ.

For a lossy dielectric, the energy losses scale with the participation ratio. Because the crystalline substrate of a wafer is a very clean dielectric, i.e. it has a low number of impurities and defects, CPWs can achieve high quality factors (about 1×10^6 for low powers) if care is taken to obtain a clean interface between metal and substrate [52]. In CPWs the capacitance that can be obtained is limited because of the separation between the central conductor and the return conductors that is usually in the order of a few µm.

The microstrip geometry relies on a single conducting track on top of a dielectric. The return conductor is provided by a large ground plane on the other side of the dielectric. The dielectric can be the substrate of a backside metalized wafer or a deposited thin film. In a microstrip the electric field is almost entirely within the dielectric, making the loss properties of the dielectric particularly important. Perfect crystalline dielectrics like silicon or sapphire wafers have proven to enable low losses in this geometry, while deposited thin films tend to show higher loss. For realizing high capacitance in this geometry, however, the case of very thin dielectric layers is most interesting. These thin films can be engineered to be only a few nm thick.

3.1.2   Quarter-Wave Resonators

The resonators used in this work, to test and demonstrate the results of the developed fabrication procedure, are $\frac{\lambda}{4}$-resonators, also called quarter-wave resonators. They consist of a transmission line of length l that is shorted to ground on one end and capacitively coupled to a feed line on the other end.

Resonance Frequencies

The geometry of a quarter-wave resonator imposes boundary conditions on the electric field in the line, namely a voltage node at the end of the resonator that is shorted to ground and a current node on the opposite side, where the circuit is open. Oscillation modes that satisfy these conditions have a voltage node at the short end of the resonator and a maximum in voltage amplitude at the open end. A schematic of this is shown in fig. 3.3a. The frequency f_r of the first mode that fulfills the boundary conditions is given by

$$f_r = \frac{1}{4l\sqrt{LC}} = \frac{v}{4l}. \tag{3.1.14}$$

Here we used the speed of light $v = \frac{1}{\sqrt{LC}}$ in a transmission line. We already derived this parameter as phase velocity in eq. (3.1.10). Interpreting eq. (3.1.14) appears simple. The resonance frequency is the inverse of the time it takes a traveling wave in this transmission line to travel four times the length of the resonator. In other words, exactly a quarter of the wavelength of a traveling wave fits inside the resonator. This justifies the name quarter-wave or $\frac{\lambda}{4}$-resonator for this kind of device. But the boundary conditions are also fulfilled by any frequency, that is an uneven multiple of the basic resonance frequency f_r. If we number them with the index i, we can write

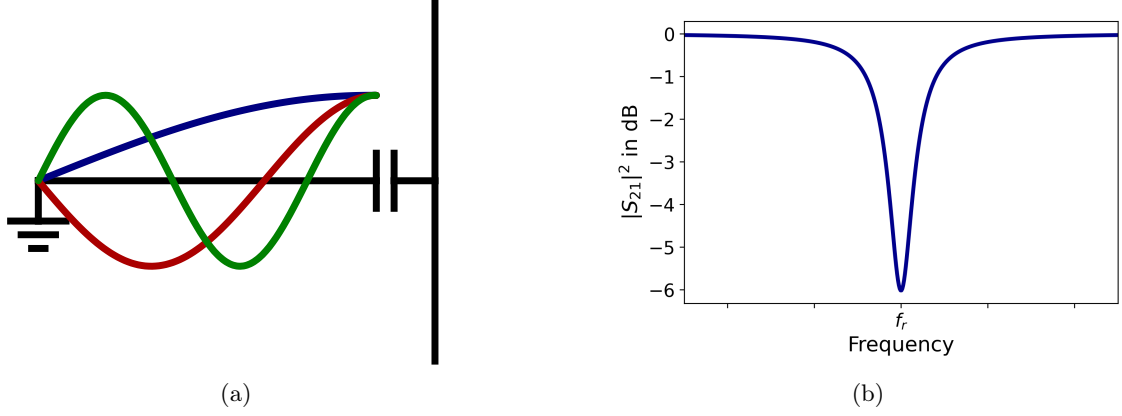$$f_i = (2i + 1) \cdot f_r. \tag{3.1.15}$$

Figure 3.3: The boundary conditions of a distributed quarter-wave resonator lead to a series of resonant modes instead of the single mode of a lumped-element resonator. **(a)** Qualitative depiction of the voltage distribution of the first three modes of a quarter-wave resonator capacitively coupled to a feed line on the right and shorted to ground on the left. **(b)** Generic form of a Lorentzian resonance dip in the transmission of a feed line that is coupled to a resonator. The form is given by (3.1.16).

Fig. 3.3a shows the voltage distribution for the basic frequency f_r, as well as for the higher modes f_1 and f_2.

Transmission Spectrum

As already mentioned, the open end of the resonator is capacitively coupled to a feed line, enabling interaction with the outside world. The coupled resonator appears in the transmission spectrum of the feed line, as drawn in fig. 3.3b. For each resonance, the squared transmission parameter $|S_{21}|^2$ shows a Lorentzian dip [41]

$$|S_{21}|^2 = 1 - \frac{D}{1 + \left(2\frac{f-f_r}{\delta_{FWHM}}\right)^2}. \tag{3.1.16}$$

The depth D and the full width at half maximum δ_{FWHM} are given by the losses of the resonator and the strength of the coupling, as will be explained in sections 3.1.3 and 3.1.4. Equation (3.1.16) only accounts for one resonance, but in a quarter-wave resonator of course each resonance adds such a dip, resulting in the transmission spectrum of a quarter-wave resonator

$$|S_{21}|^2 = 1 - \sum_i \frac{D}{1 + \left(2\frac{f-f_i}{\delta_{FWHM}}\right)^2}. \tag{3.1.17}$$

14

Lumped-Element Equivalent Circuit

A quarter-wave resonator is a distributed element, with its capacitance, inductance, and resistance not at a single point, but spread out over its length. Nevertheless, it is convenient to consider its equivalent lumped-element circuit [41, 51, 53]. We start from the input impedance of a transmission line that is shorted at one end

$$Z_{\text{in}} = Z \cdot \frac{1 - i \tanh \alpha l \cot \beta l}{\tanh \alpha l - i \cot \beta l}, \tag{3.1.18}$$

with the characteristic impedance of the transmission line Z and the propagation constants as introduced before and the length l of the shorted line. Using eq. (3.1.8) and eq. (3.1.14) we can make the connection between the propagation constant β, the probing frequency ω and the resonance frequency ω_{r}

$$\cot \beta l = \cot \omega l \sqrt{LC} = \cot \frac{\omega \pi}{2\omega_{\text{r}}} \approx -\frac{\Delta \omega}{\omega_{\text{r}}} \frac{\pi}{2}, \tag{3.1.19}$$

where the approximation is valid only around the resonance frequency ($\frac{\omega - \omega_{\text{r}}}{\omega_{\text{r}}} = \Delta\omega/\omega_{\text{r}} \ll 1$). Using this and assuming small losses ($\alpha l \ll 1$), eq. (3.1.18) simplifies to

$$Z_{\text{in}} = Z \cdot \frac{1}{\alpha l + i \frac{\Delta \omega}{\omega_{\text{r}}} \frac{\pi}{2}}. \tag{3.1.20}$$

Comparing this result to the input impedance of a parallel RLC circuit

$$Z_{\text{RLC}} = \frac{1}{1/R_{\text{le}} + 2i\Delta\omega C_{\text{le}}}, \tag{3.1.21}$$

one can identify the equivalent lumped-element circuit parameters

$$R_{\text{le}} = \frac{Z}{\alpha l} \tag{3.1.22}$$

$$C_{\text{le}} = \frac{\pi}{\omega_{\text{r}} Z} = \frac{l}{2}C. \tag{3.1.23}$$

Then, from the undamped resonance frequency of an RLC circuit ($\omega_{\text{r}} = \frac{1}{\sqrt{L_{\text{le}}C_{\text{le}}}}$) we get the equivalent lumped-element inductance

$$L_{\text{le}} = \frac{8l}{\pi^2}L. \tag{3.1.24}$$

The condition $\alpha l \ll 1$ can be understood as the requirement that the signal does not get attenuated notably during propagation through the distributed resonator. The lumped-element circuit picture is only valid around the resonance frequency, meaning that the shape of the resonance can be explained locally, but at different frequencies the two devices still behave distinctively differently. This becomes obvious considering that the lumped-element resonator has only one resonant frequency, while the distributed resonator supports higher modes as well.

The resonators we want to treat are capacitively coupled to the feed line with an extra coupling capacitor. This adds the coupling capacitance C_c, modifying the resonance frequency

$$\omega_{\mathrm{r}}' = \frac{1}{\sqrt{L_{\mathrm{le}}\left(C_{\mathrm{le}} + C_c\right)}}. \tag{3.1.25}$$

Formally, for this equation to be true, the condition $C_c^2 \omega_{\mathrm{r}}'^2 Z_0^2 / 4 \ll 1$ has to hold, however, this condition is easily fulfilled for a characteristic impedance of $50\,\Omega$ at GHz frequencies.

3.1.3 Losses and Quality Factors

Although the derivations from above use the approximation of a lossless or low-loss transmission line, losses are a significant property of a resonator. They can be quantified using the quality factor Q defined as [51]

$$Q = \omega \cdot \frac{\text{average energy stored}}{\text{energy loss/second}}, \tag{3.1.26}$$

giving a measure of the resonators' ability to preserve the energy stored in it at frequency ω. The losses arise from different sources like radiation, conduction, or, most relevant for this work, dielectric loss. These internal losses give rise to the so-called internal quality factor Q_{int} characterizing the dissipation of energy inside the resonator. Moreover, the coupling of the resonator to the outside world allows energy to be exchanged and thereby opens another loss channel from the resonators' point of view. This loss channel is characterized by the so-called coupling quality factor Q_{c}. Together with the internal quality factor Q_{int}, it combines to give the loaded Q or Q_{l}

$$\frac{1}{Q_{\mathrm{l}}} = \frac{1}{Q_{\mathrm{int}}} + \frac{1}{Q_{\mathrm{c}}}. \tag{3.1.27}$$

Using the same principle, Q_{int} itself can be separated into the different contributions as mentioned above. Especially for the dielectric loss it is common to introduce the loss tangent $\tan \delta_{\mathrm{diel}} = \frac{1}{Q_{\mathrm{diel}}}$ as the reciprocal of the dielectric quality factor Q_{diel}.

3.1.4 Circle Fit

The parameters of a resonator can be obtained from its transmission spectrum. We already introduced the transmission parameter S_{21} of a feed line coupled to a resonator in eq.(3.1.16) and visualized it in fig. 3.3b. In terms of quality factors it can be expressed as

$$S_{21}(f) = 1 - \frac{\frac{Q_{\mathrm{l}}}{Q_{\mathrm{c}}}}{1 + 2iQ_{\mathrm{l}}\frac{f - f_{\mathrm{r}}}{f_{\mathrm{r}}}}. \tag{3.1.28}$$

Methods used to fit this equation to the spectrum are referred to as circle fits because of the real and imaginary part of the transmitted signal around the resonance forming a circle in the complex plane. The method used for the analysis in this thesis was already implemented in other works of the group [54]. To account for the influence of the environment, especially the measurement setup,
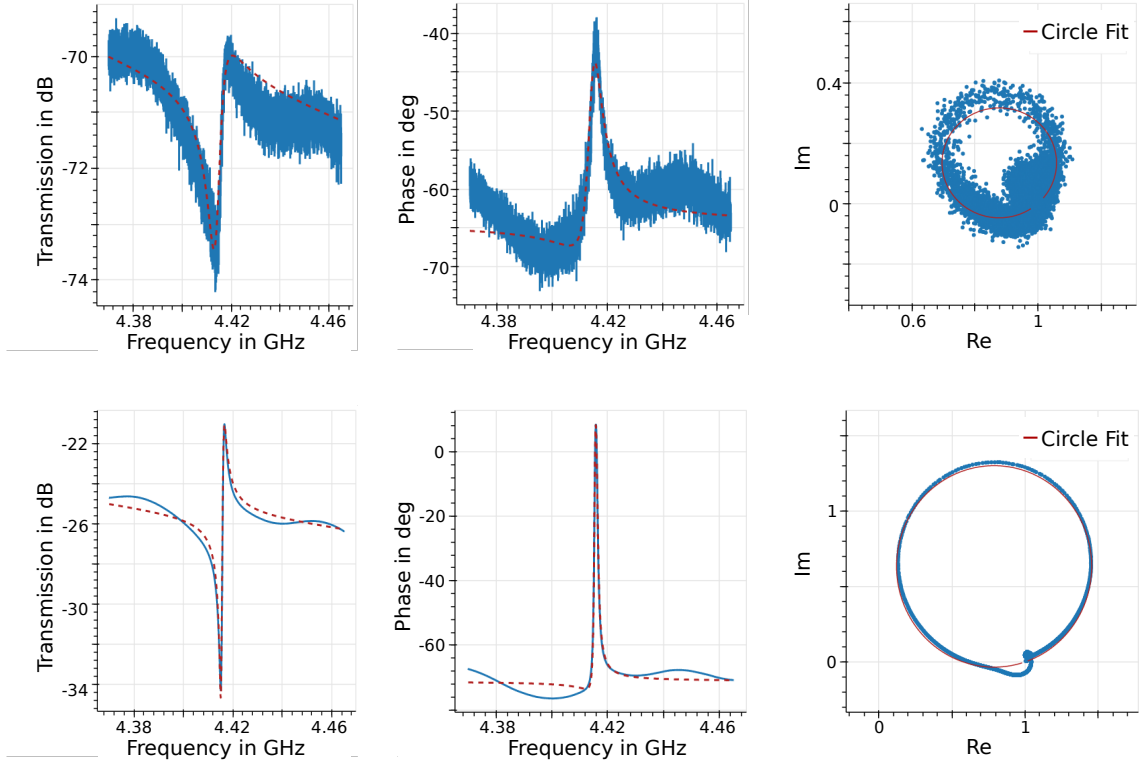
Figure 3.4: Exemplary resonance measurements with circle fit used for analysis. The top row is taken at low power, the bottom row at high power. **from left to right:** signal magnitude, phase and normalized signal in the complex plane.

eq. (3.1.28) is extended to

$$S_{21}(f) = \left(ae^{i\varphi}e^{-2\pi i f\tau}\right)\left(\left(1 - \frac{\frac{Q_\mathrm{l}}{Q_\mathrm{c}e^{i\phi_0}}}{1 + 2iQ_\mathrm{l}\frac{f-f_\mathrm{r}}{f_\mathrm{r}}}\right),\right. \tag{3.1.29}$$

including factors for global attenuation and phase shift $(ae^{i\varphi})$, a phase shift linear in frequency $(e^{-2\pi i f\tau})$, and the phase offset ϕ_0, capable of accounting for impedance mismatch before and after the resonator. The fit parameters that were extracted from transmission data in this thesis are the resonance frequency as well as the internal and coupling quality factors.

Fig. 3.4 shows exemplary measurements of a resonator coupled to a feed line with the corresponding circle fit for two different signal powers. For both, the fit captures the resonant feature in the center of the shown data, while failing to describe its surroundings. This is because of background variation mainly caused by standing waves forming due to reflections along the feed line. Giving a quantitative estimate for the errors of the fitting parameters is therefore challenging. The errors that are presented as error bars later in the analysis do only represent the statistical uncertainty of the fits. If, like from the top to the bottom row in fig. 3.4, the noise level of the measurement is reduced, these statistical errors get smaller, while the uncertainty introduced by the background variation remains. This has to be taken into consideration when interpreting the results presented later in chapter 6.

3.1.5 Average Photon Number

With knowledge of the quality factors of a resonator and the incident power, it is possible to calculate the average photon number $\langle n_{\mathrm{ph}} \rangle$ in the resonator. Following the calculation from [55], we start by considering the incident power P_{inc} on the feed line at the coupled resonator. It can be reflected as P_{refl}, transmitted as P_{trans} or absorbed by the resonator as P_{abs}

$$P_{\mathrm{inc}} = P_{\mathrm{refl}} + P_{\mathrm{trans}} + P_{\mathrm{abs}} = P_{\mathrm{inc}}|S_{11}|^2 + P_{\mathrm{inc}}|S_{21}|^2 + P_{\mathrm{abs}}. \tag{3.1.30}$$

Here we already plugged in the definition for reflected and transmitted power in terms of scattering parameters. The scattering parameters of a resonator that shunts the feed line are given by [56]

$$S_{21} = \frac{Q_{\mathrm{c}}}{Q_{\mathrm{c}} + Q_{\mathrm{l}}} \tag{3.1.31}$$

$$S_{11} = \frac{-Q_{\mathrm{int}}}{Q_{\mathrm{c}} + Q_{\mathrm{l}}}, \tag{3.1.32}$$

with the different quality factors as described above. This we can now use to express the absorbed power in terms of the quality factors of the resonator

$$P_{\mathrm{abs}} = \frac{2Q_{\mathrm{l}}^2}{Q_{\mathrm{c}}Q_{\mathrm{int}}}P_{\mathrm{inc}}. \tag{3.1.33}$$

The absorbed power can be attributed entirely to the internal losses of the resonator. These are simply given by the amount of energy stored in the resonator $E = \langle n_{\mathrm{ph}} \rangle \hbar \omega_{\mathrm{r}}$ and the internal loss rate κ_{int}

$$P_{\mathrm{abs}} = \langle n_{\mathrm{ph}} \rangle \hbar \omega_{\mathrm{r}} \kappa_{\mathrm{int}}. \tag{3.1.34}$$

Using the definition of the internal quality factor stated in eq. (3.1.26), inserting E for the stored energy and κ_{i} for the loss rate, we obtain

$$P_{\mathrm{abs}} = \langle n_{\mathrm{ph}} \rangle \frac{\hbar \omega_{\mathrm{r}}^2}{Q_{\mathrm{int}}}, \tag{3.1.35}$$

which in combination with eq. (3.1.34) yields the final expression for the average photon number

$$\langle n_{\mathrm{ph}} \rangle = \frac{2Q_{\mathrm{l}}^2}{Q_{\mathrm{c}}\hbar \omega_{\mathrm{r}}^2}P_{\mathrm{inc}}. \tag{3.1.36}$$

It has to be noted, that this result does not account for feed line mismatch and other reflections in the measurement line and can therefore be interpreted as an upper bound on the number of photons in the resonator [55].

3.2 Superconductivity and Kinetic Inductance

Superconductivity is an effect that occurs in some materials at very low temperatures. When below a critical temperature T_c these materials completely lose their electrical resistance and expel magnetic fields. Superconductivity has many applications and notably offers an essential tool for building high magnetic field applications, such as particle accelerators or magnetic resonance imaging (MRI), or a promising candidate for lossless power transfer.

Another aspect of superconductivity is its importance in the field of quantum physics. Superconducting qubits are a promising platform for the implementation of a quantum computer and superconducting detectors are state of the art in the field of microwave astronomy. In this section, we will focus on the elements of superconductivity that are relevant for this thesis, namely the Meissner effect and kinetic inductance. A detailed treatment of superconductivity, its phenomena, and the different theories used to describe it can be found in [38].

3.2.1 Meissner Effect

The expelling of the magnetic field from the superconducting material is known as the Meissner effect. The magnetic field decays exponentially from the surface of the superconductor to its inner region on a length scale, referred to as the London penetration depth λ. At zero temperature it is given by

$$\lambda = \sqrt{\frac{mc^2}{4\pi n_s e^2}}, \tag{3.2.1}$$

where m is the electron mass, c the speed of light, n_s the superconducting electron density and e the elementary charge.

3.2.2 Kinetic Inductance

Kinetic inductance arises from the kinetic energy of the charge carriers in contrast to classic magnetic inductance which comes from the energy stored in the magnetic field induced by the current [57, 58].

Intuitive Picture

To motivate kinetic inductance, one can picture a conductor with length l and cross-section A supporting a current I. The charge transport is done by charge carriers with mass m, charge q, and assumed homogeneous number density n. A sketch of such a conductor is shown in fig. 3.5. We can easily find the expressions relating the current to the average drift velocity v of the charge carriers.

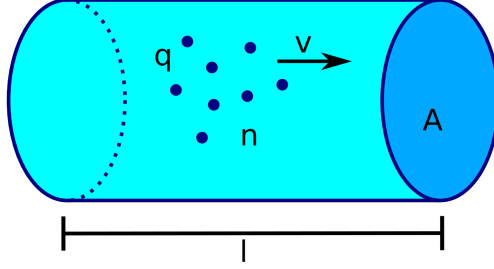$$I = vqnA \iff v = \frac{I}{qnA} \tag{3.2.2}$$

Figure 3.5: Sketch of charge transport in a wire. Charge carriers of charge q and number density n move with an average drift velocity v through a conductor of length l and cross-section A.

If we assume, that all charge carriers are moving at the average drift velocity, this results in the kinetic energy

$$E_{kin} = \frac{m\left(\frac{I}{qnA}\right)^2}{2} \cdot nAl = \frac{ml}{nAq^2} \cdot \frac{I^2}{2}. \tag{3.2.3}$$

Comparison with the energy of an inductive element $E_{kin} = \frac{1}{2}LI^2$ then leads to the kinetic inductance

$$L_{kin} = \frac{ml}{nAq^2}. \tag{3.2.4}$$

While this approach is only an intuitive picture for where kinetic inductance comes from, it still gives the correct proportionalities on the geometric factor $\frac{l}{A}$ and on the material parameters $\frac{m}{nq^2}$. For normal conductors, the reactive part of the characteristic impedance coming from kinetic inductance vanishes compared to the resistive part up to THz frequencies [58]. For superconductors, however, the resistance vanishes and therefore kinetic inductance can dominate.

Temperature Dependence

An important point for this thesis is the temperature dependence of the kinetic inductance. An increase in temperature leads to both, a direct decrease in the number of charge carriers due to thermal breaking of Cooper pairs and the formation of quasiparticles and secondly the increase of the penetration depth λ which again leads to a decrease in charge carrier density. The specific dependencies can be worked out using the Mattis-Bardeen theory [59].

For this work, especially the dependence of the resonance frequency of a resonator on the temperature T is important. An approximate formula can be found for the change in frequency $\delta f_{\mathrm{r}} = f_{\mathrm{r}}(T) - f_{\mathrm{r}}(T=0)$ [53, 60]

$$\frac{\delta f_{\mathrm{r}}}{f_{\mathrm{r}}(T=0)} = -\frac{\alpha}{2}\sqrt{\frac{\pi\Delta}{2k_{\mathrm{B}}T}}\exp\left(-\frac{\Delta}{k_{\mathrm{B}}T}\right). \tag{3.2.5}$$

Here α gives the kinetic inductance fraction of the resonator and Δ is the superconducting gap of

the superconductor at zero temperature. Later in this thesis, we will use this formula to extract information about the kinetic inductance fraction α from measurements at different temperatures.

Nonlinearity

For quantum physics and especially for the construction of quantum-limited parametric amplifiers kinetic inductance is interesting because of its nonlinearity. Coming from a different direction than our intuitive treatment before, namely using BCS theory one can show that the kinetic sheet inductance $L_\square = L$ of a thin superconducting film is given by [61]

$$L_\square = \frac{\hbar R_\square}{\pi \Delta}. \tag{3.2.6}$$

Here, Δ denotes the superconducting gap at zero temperature and $R_\square$ is the normal state sheet resistance. For thin-film circuits inductance and resistance are often given per square (shown with the $\square$ in the subscript). This comes from the geometric scaling of these values. As they are proportional to the length of a conductor and inversely proportional to its width, each square of material, independent of its size has the same inductance or resistance.

The dependence of the kinetic inductance on the superconducting energy gap Δ gives rise to its nonlinearity. This is because Δ depends on the supercurrent flowing through the conductor. The kinetic energy of the charge carriers reduces the condensation energy of the superconductor [61].

The connection between kinetic inductance and normal state resistance, as given by eq. (3.2.6) implies, that superconductors with large normal state resistance also have large kinetic inductance. Disordered superconductors, such as granular aluminum (grAl) [62, 63] are therefore ideal candidates for building high kinetic inductance nonlinear devices. Examples of such devices are parametric amplifiers, as will be discussed in the next section.

3.3 Quantum-Limited Amplifiers

Quantum-limited parametric amplifiers have become essential in the fields of quantum information, computing, and research and do also find diverse applications in building detectors for astronomy or the search for dark matter.

Those devices offer significant amplification for low power signals while only adding noise close to the quantum limit of amplification. Used as the first element of an amplification chain they are able to reduce the noise level, previously limited by the performance of semiconductor amplifiers. The higher noise of the following stages gets less relevant as the noise of an amplification chain is determined only by its first stage if the gain of this first stage is sufficiently high [51]. However, despite their fantastic potential and the many problems that have already been overcome, the application of quantum-limited amplifiers is still limited by a few drawbacks. In the following, we will give a brief overview of the basic principle of parametric amplification and then discuss the two

fundamental designs for quantum-limited amplifiers and the connected limitations and challenges.

3.3.1 Parametric Amplification

Parametric amplification is based on the principle of wave-mixing, a process that occurs in nonlinear media. The most prominent example of nonlinear mixing processes can probably be found in the field of optics [35, 36]. Nonlinear optical fibers can be used for example to convert a laser beam to a higher frequency, by combining two photons at a low frequency into one photon at double that frequency. More generally speaking, energy can be exchanged between different modes of oscillation by interaction through the nonlinear medium. This enables amplification, as energy can be converted from a pump tone to a weak signal tone. Parametric amplification processes are classified into two categories, three-wave mixing (3WM) and four-wave mixing (4WM), which differ by the number of photons involved in the process. In 3WM amplification processes, a pump photon at frequency f_p is converted into two photons at lower frequency, labeled signal (f_s) and idler (f_i). For 4WM processes, two photons of the pump are converted into signal and idler. The relations of energy conservation that have to be fulfilled are

$$f_p = f_s + f_i \quad \text{(3WM)} \tag{3.3.1}$$

$$2f_p = f_s + f_i \quad \text{(4WM)}. \tag{3.3.2}$$

However, this effect does not only occur at optical frequencies but can also become relevant in the microwave regime. A more detailed description of this interaction process can for example be found in [64].

The presence of a nonlinear medium is essential for mixing processes. Such a medium can be engineered using the nonlinearity of kinetic inductance, that was explained before in section 3.2.2.

3.3.2 Resonant Parametric Amplifiers

The first microwave parametric amplifiers (paramps) were realized in a one-port resonant design, where the signal enters a nonlinear resonator that is pumped by a strong microwave tone. The signal gets amplified by conversion of pump to signal photons and then leaks out through the input port. Using parametric amplifiers, near-quantum-limited noise performance could be achieved and used for example to observe quantum jumps of a qubit in real-time [65]. While extremely useful for many purposes, resonant paramps also exhibit significant weaknesses linked to their design as resonators. The usability of such devices is fundamentally limited by the so-called gain-bandwidth product, setting a limit to signal gain and bandwidth. Large values in both those quantities cannot be achieved simultaneously [10].

3.3.3 Traveling Wave Parametric Amplifiers

Many of the limitations of paramps, like the limited gain-bandwidth product, can be overcome by traveling wave parametric amplifiers (TWPAs) [17]. Instead of a resonant design, TWPAs are nonlinear transmission lines in which the signal is amplified while traveling through it, very similar to fiber optical amplifiers [35]. Due to this geometry of TWPAs, they do not suffer from a fundamental limitation on their gain-bandwidth product but impose new challenges.

To obtain sufficient gain across the device, a practice known as phase matching becomes important. The amplification gain becomes maximal when the phase mismatch, i.e. the difference of the wave vectors involved in the mixing process, vanishes.

$$k_p = k_s + k_i \quad \text{(3WM)} \tag{3.3.3}$$

$$2k_p = k_s + k_i \quad \text{(4WM)} \tag{3.3.4}$$

This ensures that the signal waves that are created over the whole transmission line remain in phase and constructively interfere at the end of the amplifier. Because of the nonlinearity of the transmission line this condition is not easy to fulfill over a wide bandwidth.

Typically, other mixing processes, such as the generation of higher harmonics of the pump tone, dominate over the amplification of the small signal tone if no care is taken to suppress them. These processes can lead to pump depletion [66]. The generation of higher harmonics can be suppressed by introducing a bandgap into the dispersion relation of the transmission line. This technique known as dispersion engineering can be realized by either introducing periodic loading patterns [19–22, 28, 30–34] that create a photonic crystal preventing the propagation of specific frequencies, or by including resonators along the transmission line [23, 24] leading to the same effect. The introduction of nonlinear dispersion into the TWPA is also necessary to avoid the generation of shock waves in the device, which otherwise would make significant gain impossible [67].

It is important to note that dispersion engineering can also be used to combat the problem of phase matching. By again loading the transmission line with periodic structures the dispersion relation of the line can be altered to ensure phase matching of pump, idler, and signal over wider bandwidths.

Another problem to be thought of is impedance matching. To obtain sufficient amplification in a non-resonant design and on feasible length scales, large kinetic inductance is required. As already discussed in chapter 2 different approaches were taken to either mitigate the negative effects of the increased characteristic impedance or to compensate for the increased inductance by increasing the capacitance accordingly. The second approach has the additional benefit of reducing the speed of light $v = \frac{1}{\sqrt{LC}}$ in the transmission line even more and thereby increasing the effective interaction length for the wave mixing. However, providing large additional capacitance typically comes at the price of increased loss, due to the dielectrics used to realize it. As already discussed above, the thin-film dielectrics, which are often used to achieve large capacitance, usually exhibit high losses

compared to the thick crystalline wafer substrates. It is worth noting that this problem does not apply in the same way to resonant paramps, as because of their resonant one-port design, impedance matching is not an issue. Consequently, the kinetic inductance does not have to be compensated with additional capacitance and no need for lossy dielectrics arises.

To conclude, the noise introduced by dielectric losses is one of the last remaining issues preventing true quantum-limited TWPAs. So in order to achieve low-noise broadband amplification, finding a method of constructing low-loss nonlinear transmission lines for TWPAs is a promising research goal.

Chapter 4

Fabrication

In the previous chapters, we motivated why transmission lines with high capacitance and low losses would be a significant step forward in the development of microwave traveling wave parametric amplifiers. Also, we have introduced the concept of a vacuum-gap microstrip that promises these properties. In this chapter, we will explain in detail how the vacuum-gap microstrip can be realized using nano-fabrication techniques. To do that, we will start with a general introduction to nano-fabrication and give short explanations of the most common techniques used. After that, the fabrication process developed during this master thesis will be discussed step by step. Subsequently, challenges encountered during the development of said process will be highlighted together with the strategies and measures that were used to overcome them. Finally, ideas on how to further improve the current process will be given.

4.1   Basic Concepts of Fabrication

Micro- and nano-fabrication is a fundamental ingredient of modern technological society as nano-fabricated chips are integrated into many devices of daily use. Fundamentally there are two ways to do micro- or nano-fabrication. The "bottom-up" technique is characterized by starting from an empty substrate and layer by layer building up the final structure, i.e. depositing material where one wants them to be. Doing the opposite, namely depositing material on the whole surface and then removing it where one does not want it to be, is referred to as the "top-down" technique. Both techniques rely on different material deposition and lithography methods. Therefore, in this section, we will introduce the most common ones with a focus on aspects that will be relevant later in the thesis. A wider and much more detailed treatment of micro- and nano-fabrication technology can be found in [68].

4.1.1 Material Deposition

Material can be deposited on a wafer in a variety of different ways. In this work, we used sputter deposition and electron-beam evaporation. Although there are other methods to deposit thin layers of material on a substrate, we will focus here on these two.

In sputter deposition, a target is hit by high energetic ions (usually argon) leading to the ejection of atoms from the target material which are then redeposited on the wafer. To generate these ions, a DC- or RF-field is applied between the target and a counter-electrode in a low-pressure argon atmosphere. In the resulting plasma, the positive argon ions are accelerated towards the target where they transfer their momentum to the atoms of the target ejecting them from the surface.

The second method mentioned is to heat the target to temperatures where the material evaporates from the target and then condensates on the substrate. To do that, often an electron beam is used to heat the target locally.

A main difference between these two deposition methods is that evaporated atoms are intrinsically hot as the material has to reach its temperature of evaporation. So when evaporated atoms deposit on a surface, they form their lattice structure while still hot. When the layer cools down, the film can exhibit considerable tensile stress due to thermal contraction (see also section 4.3.3). Sputtered atoms are generally cooler during deposition but nevertheless, some stress in the deposited film might appear.

A big advantage of sputter deposition is the much greater level of control that can be exerted on the film properties by variation of the process parameters. Film properties can be modified by changing parameters like bias voltage or argon pressure. Also, the substrate can be heated, affecting the crystalline structure of some deposited materials. Coming back to the issue of tensile stress, it is important for this work to note, that the strain of sputtered thin films can be controlled with the pressure of the argon in the chamber (e.g. [69]).

Because of the high vacuum necessary for evaporation and the argon plasma needed for sputtering, a defining difference between the two processes is also directionality. For evaporation, the material deposits only in the direct line of sight from the target. For sputtering, due to the presence of the argon plasma, deposition is generally more isotropic while also depending on the process parameters. This becomes relevant for example for the shadow effect discussed in the following section on lift-off.

Other differences to be named are generally slower deposition speeds for sputtering and a much narrower range of compatible materials for evaporation. While evaporation is mostly limited to pure metals, sputtering is capable of depositing a wide range of materials, also including non-metals, alloys, ceramics, and polymers.

4.1.2 Lithography

In the context of micro- and nano-fabrication, lithography describes the process of transferring an image or pattern to a polymer thin film called a resist. This resist is previously deposited as a continuous layer on a substrate, such as a wafer. Different methods can be used to achieve this pattern transfer.

In electron-beam lithography, a focused beam of electrons is used to pattern structures in an electron-sensitive resist. Exposure to electrons changes the chemical properties of the resist depending on its specific composition. One can distinguish between positive and negative resists. In positive resists, the exposure leads to solubility in a chemical reactive. In negative resists, it leads to crosslinking of the resist molecules resulting in the opposite effect. Negative resists lose their solubility where they are exposed. The removal of the soluble parts of the resist film in the chemical reactant is referred to as development.

Other methods of lithography are focused-ion-beam lithography and optical lithography. The latter mainly uses light of the blue and ultraviolet parts of the electromagnetic spectrum to manipulate the chemical properties of the resist. Instead of walking a localized beam across all the areas of the wafer that should be exposed, optical lithography also offers the possibility to use fabricated masks between the wafer and a light source to expose samples in a much shorter time.

Without regard to the method of their creation, thin films of patterned resist can be used to make changes to the surface of a wafer, either by etching or by material deposition followed by lift-off. Although the sketches from fig. 4.1 and fig. 4.2 both show a positive resist being used, both positive and negative resists can be used for both processes.

4.1.3 Lift-Off

One method of using a resist mask to pattern structures on a wafer is lift-off. A layer of the desired material is deposited on top of an already exposed and developed resist mask. At the mask openings, the material can reach the surface of the wafer and deposit on it; in all areas covered by resist, the material deposits on top of the resist film. After deposition, the wafer is dipped in a solvent that dissolves the resist, only leaving metal on the areas that were not covered by the resist mask. As shown in figs. 4.1a to 4.1c, the first step of a lift-off process is the deposition, exposure, and development of the resist film on top of the substrate. This is followed by material deposition before finally the resist film is dissolved in a solvent (usually Acetone or NMP), leaving a metal layer formed according to the lithography pattern.

Important factors for successful lift-off are a directional material deposition method such as evaporation and an undercut in the resist profile. The problem with a resist profile that does not have an undercut or even shows a sloped profile is depicted in fig. 4.1d. The metal that is deposited on the wafer surface is connected to the metal deposited on the resist due to metal deposition on
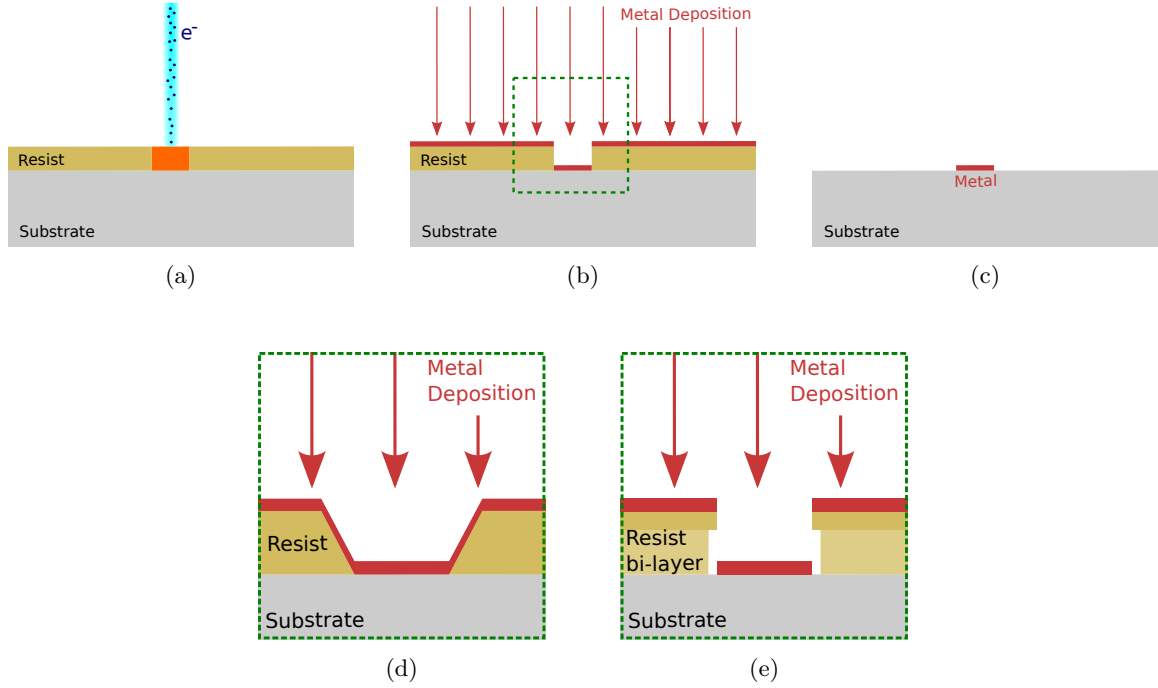
Figure 4.1: Schematic of a positive resist electron-beam lift-off process. **(a)** First the resist film is exposed by a focused electron beam. **(b)** After the development of the resist (here a positive resist) one can evaporate metal on the wafer. **(c)** Finally, the resist is removed using a solvent leaving only the metal on the exposed areas on the wafer. A negative resist would leave metal everywhere except the exposed areas. **(d)** A vertical or even sloped resist profile leads to a connection of the deposited metal on the bottom of the trenches with the metal on top of the resist. **(e)** Undercut profiles can be achieved using resist bi-layers. The resulting shadow effect prevents step coverage of the resist.

the sloped resist wall, making lift-off significantly harder or even impossible. A common way to achieve an undercut is to use resist bi-layers as shown in fig. 4.1e. Usually, the layers are chosen such that the lower layer is easier removed by the developer than the top layer. During development part of the lower resist layer is washed away under the one on top. The resulting shadowing effect makes coverage of the resist step by directional material deposition impossible, ensuring unhindered removal of the material on top of the resist mask. Another way the shadowing effect can be used is for example in the fabrication of Josephson junctions in the double angle evaporation or Dolan bridge technique [70].

4.1.4 Etching

Being the standard technique for pattern transfer in the semiconductor industry, etching is an important part of micro- and nano-fabrication. On top of a pre-deposited material, a resist mask is created by lithography. After that, the whole wafer is dipped into a chemical solution (wet etch) or exposed to a plasma (dry etch) which etches the underlying material. Where the material was covered by the resist mask, it is protected, while where the etchant can access it, it is removed. A distinctive difference between wet and dry etch is that wet etches are usually isotropic while dry etching with plasma can be very directional.

Fig. 4.2 shows a sketch of a masked plasma-etch process of a metal layer with a positive protective
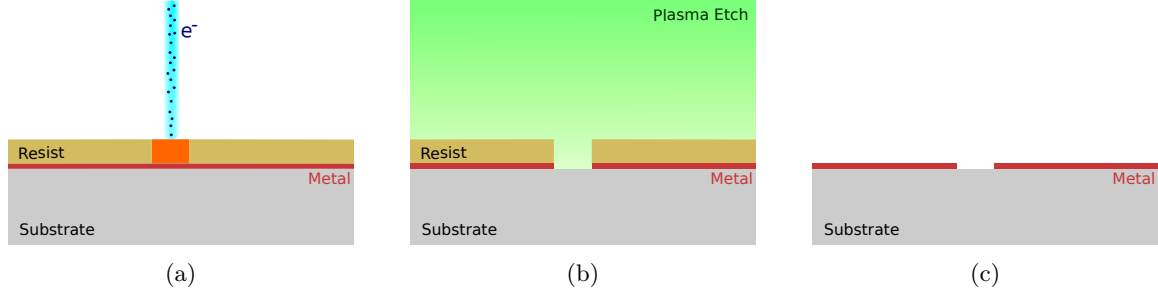
Figure 4.2: Schematic of a positive resist masked plasma etching process using electron-beam lithography. **(a)** A pre-deposited metal layer is coated by a resist that is then exposed by a focused electron-beam. **(b)** After the development of the here positive resist the sample is exposed to a plasma etch that removes the metal where it can access it. **(c)** Finally the protective resist is removed by either a solvent or by a different plasma (usually O_2 ashing)

.

resist mask. First, the metal layer that is already in place is coated by a resist film. This resist (here again a positive resist) is exposed by an electron beam (fig. 4.2a) and developed. The whole sample is exposed to a plasma etch (fig. 4.2b) that removes the metal where it is not protected. The final result, after removal of the protective resist, can be seen in fig. 4.2c.

## 4.2   Vacuum-Gap Microstrip Fabrication Process

The development of the new vacuum-gap microstrip fabrication process is the main achievement of this work. The process of constructing a vacuum-gap microstrip can be separated into the five steps shown in fig. 4.3: deposition of the base layer, patterning of the sacrificial resist as a place holder for the tunnel, deposition of the ground plane on top of the sacrificial resist, etching of the ground plane and finally removal of the sacrificial resist from the tunnels.

4.2.1   Base Layer

The main part of the fabrication starts with the patterning of the base layer. It is patterned in aluminum using an MMA-PMMA bi-layer lift-off process. Like in all following layers we use electron-beam lithography to pattern the resist. The wafer is then developed in a mixture of isopropanol and water, rinsed in water and blow-dried with nitrogen. A 40 nm layer of aluminum is deposited via electron-beam evaporation and lifted off in an acetone bath under ultrasonication. The step is completed with rinsing in isopropanol and again drying in N_2. Fig. 4.4 shows optical microscope images of the finished layer. The white areas are aluminum, the gray background is the silicon substrate.
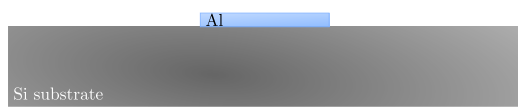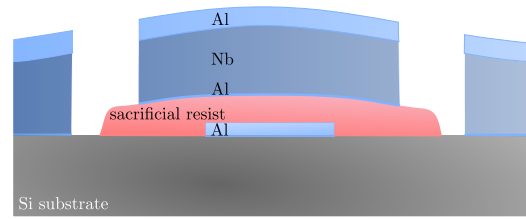
(a) Base conductor deposition
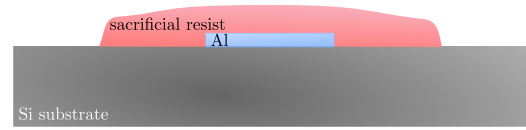
(b) Sacrificial resist patterning
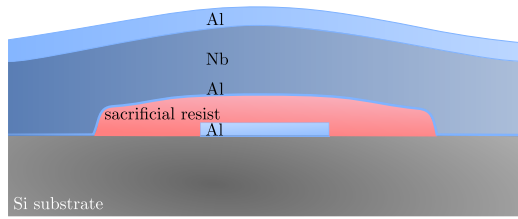
(c) Ground plane deposition

(d) Hole etching
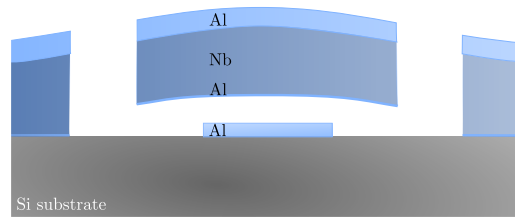
(e) Sacrificial resist removal

Figure 4.3: Basic sketch of the fundamental steps of the developed fabrication process. **(a)** The base conductor layer is deposited. **(b)** Thin lines of sacrificial resist are patterned to act as a place holder for the tunnels. **(c)** The ground plane is deposited on top of the sacrificial resist. **(d)** Holes are etched into the ground plane so that the sacrificial resist becomes accessible. **(e)** The sacrificial resist is removed from the tunnels with an oxygen plasma.

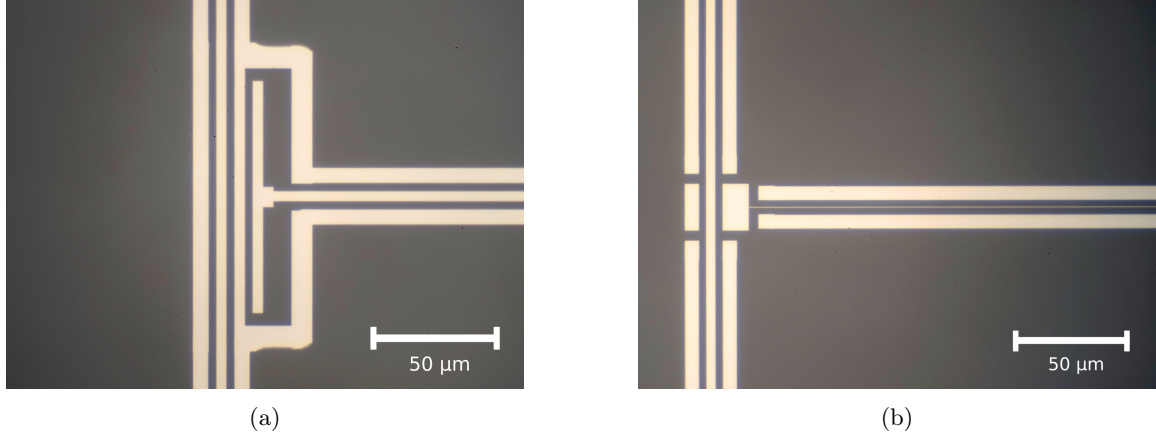Figure 4.4: Microscope images after the first fabrication step. The aluminum appears white, the silicon substrate gray. **(a)** CPW resonator (extending to the right) coupled via a coplanar coupler to a CPW feed line (vertical). **(b)** Vacuum-gap microstrip resonator (extending to the right) coupled via a parallel-plate coupler (only foundations present at this step) to a CPW feed line (vertical).

4.2.2 Sacrificial Resist Layer

The next step is the patterning of the sacrificial resist to form the tunnels of the vacuum-gap microstrip resonators and the air-bridges. As the resist should stay only on the wafer where there should be tunnels or bridges, we use a negative resist (ma-N 2401 supplied by *micro resist technology*). The resist is deposited via spin coating at 4000 rpm to obtain a film thickness of approximately 80 nm on flat surfaces. The patterning is again done using electron-beam lithography. Afterward, the sample is developed in a diluted metasilicate-based developer, rinsed in water, and blow-dried with nitrogen. The metasilicate developer is chosen because unlike other alternatives based on TMAH it does not etch aluminum. Photographs of the sample after development are shown in fig. 4.5. To ensure continuous metal coverage at the next step, we form a smoother inner profile of the tunnels by overexposing the resist. By the proximity effect, the exposed lines become wider and the flanks of the developed resist become sloped and rounded. The results are similar to the resist profile in fig. 4.1d, but rather than being a problem, the continuity of the metal layer that will be deposited in the next step is an essential requirement for the success of the fabrication. While more clearly visible in the AFM analysis of the sample (see section 6.1.2), the sloped wings also appear in the optical images as lighter blue shadows at the borders of the resist lines.

4.2.3 Ground Plane Deposition

The fabrication process continues with the deposition of the ground plane on top of the sacrificial resist. The ground plane is made up of a triple layer of 10 nm of aluminum as the lowest layer, followed by 200 nm of niobium and terminated by 50 nm of aluminum. This tri-layer structure is necessary to meet a series of requirements that the ground plane has to fulfill. These are etching selectivity, the creation of a hard mask for etching, and protection against undesired oxides. The detailed line of thinking on that issue is outlined in section 4.3.3. The niobium layer is deposited using sputtering while the aluminum is evaporated. The three steps are done in the same machine
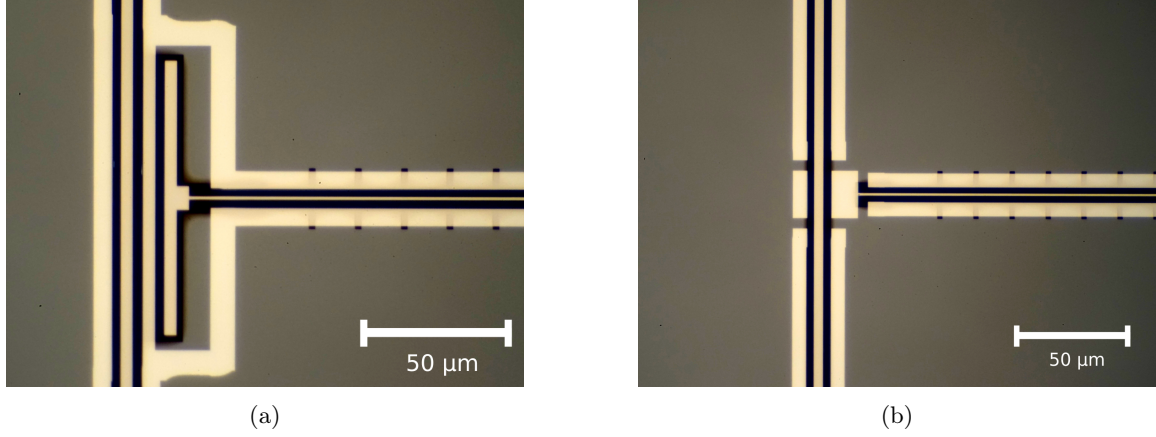
Figure 4.5: Microscope images after the sacrificial resist deposition. Aluminum appears white, the silicon substrate gray and the sacrificial resist black where it is on top of the silicon substrate. On top of the aluminum, it is hardly visible. **(a)** CPW resonator (extending to the right) coupled via a coplanar coupler to a CPW feed line (vertical). **(b)** Vacuum-gap microstrip resonator (extending to the right) coupled via a parallel-plate coupler (only foundations present at this step) to a CPW feed line (vertical).

without exposure to the atmosphere in between, avoiding the formation of oxides between them. To ensure full coverage of the sacrificial resist by the innermost layer, the sample is rotated during the deposition of the inner aluminum layer at an angle of 30°.

4.2.4   Hole Etching

To access and finally remove the sacrificial resist from beneath the ground plane, holes are patterned and etched as access points to the tunnels. The structures patterned include the hole arrays on top of the microstrip tunnels as well as larger patches to remove the ground plane on top of the CPW lines, resonators, and coplanar couplers (see chapter 5). The couplers in parallel-plate geometry are created by patterning a frame around them separating them from the ground plane. The hole creation process is composed of multiple plasma etching steps shown in fig. 4.6. The first step is to form the topmost aluminum layer into a hard mask using a positive protective resist. Then the wafer is diced into individual chips before the etching is continued to protect the chips. The next step is to etch through the niobium and then through the thin aluminum layer, before removing the sacrificial resist with an oxygen plasma.

In the first etching step, we etch the aluminum layer with a BCl_3 plasma. For masking we use the positive CSAR-62 resist from *Allresist* as it is able to withstand the BCl_3 plasma for long enough to etch through the aluminum, creating a hard mask for the following etching step (see fig. 4.6a). Optical microscope pictures are shown in fig. 4.7. The etching of the aluminum is followed by a short CF_4 conversion step to avoid excessive post-etching corrosion of the aluminum [71, 72]. Unfortunately, corrosion due to the presence of chlorine on the surface could not be entirely avoided, as can be observed in fig. 4.8. The resist mask is then removed by oxygen plasma ashing, leaving the aluminum layer as a hard mask for further processing.
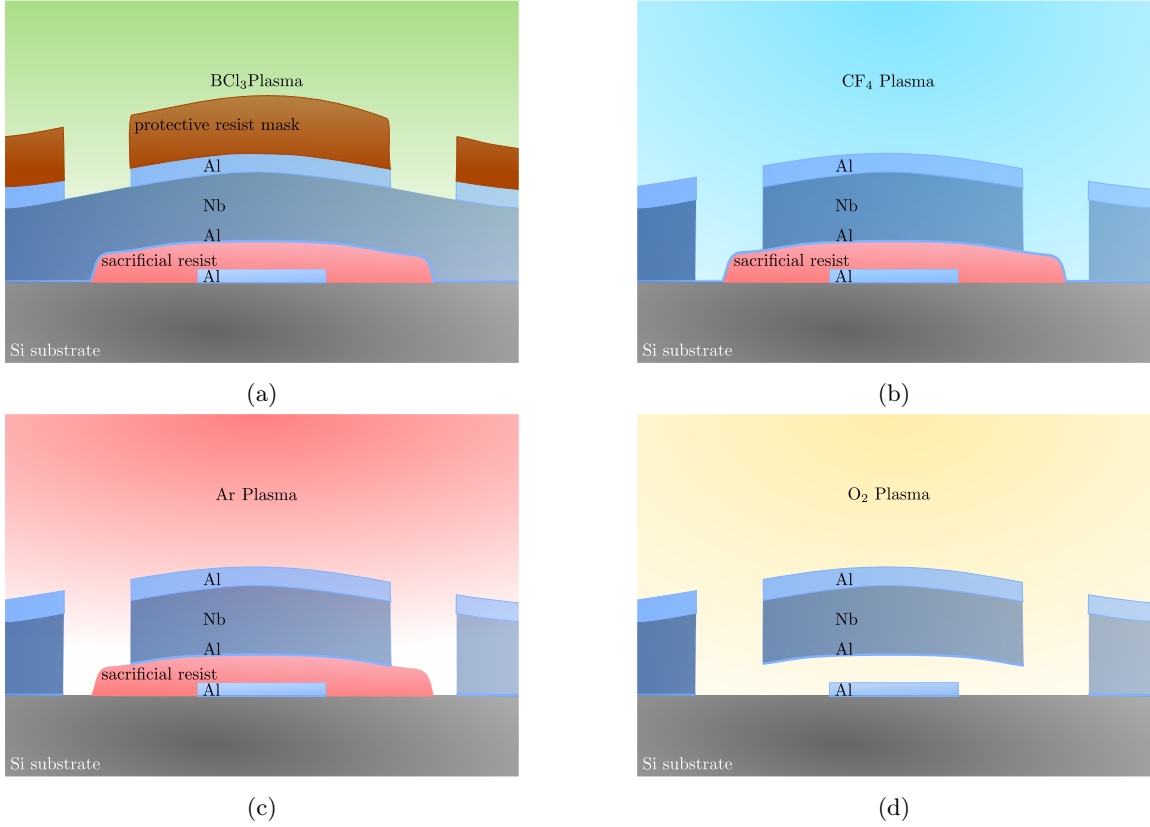
Figure 4.6: The four etching steps to create the access points to the resist through the ground plane and remove the sacrificial resist. **(a)** BCl_3 plasma etching of the aluminum top layer of the ground plane masked by a protective resist mask. **(b)** CF_4 plasma etching of the niobium layer. The upper aluminum layer works as a mask for this process. **(c)** Ar milling of the innermost aluminum layer. **(d)** O_2 plasma etch of the sacrificial resist.

At this point, the wafer is diced using a laser cutter (see section 4.3.5) and from that point on the three chips on the wafer can be treated separately. Dicing is done at this point in the fabrication process to have the tunnels still filled with the sacrificial resist and covered by a continuous ground plane. Firstly that makes it possible to protect the chip with a layer of protective resist from any damage from particles generated by the dicing process. Secondly, the sacrificial resist inside the tunnels protects them from collapse due to inevitable vibrations. The dicing is done in two steps while for each step the wafer is glued to a copper support stencil to avoid shattering of the wafer during dicing.

After the dicing, we continue the etching of the ground plane. Masked by the aluminum the niobium layer of the ground plane is etched with a CF_4 plasma down to the last, only a few nm thick aluminum layer (see fig. 4.6b). To protect the aluminum of the base layer, this last barrier is removed solely by argon milling (see fig. 4.6c) as experiments with BCl_3 etching have shown extensive damage to the underlying structures of the base layer.
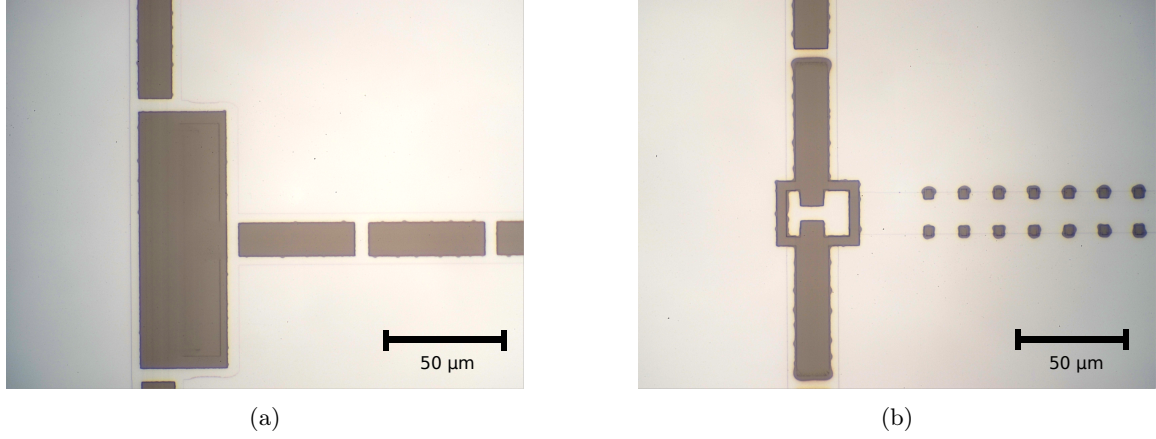
Figure 4.7: Microscope images of the sample after the etching of the outer aluminum layer of the ground plane. The aluminum mask appears bright, the underlying niobium gray. Some etching defects are visible at the edges of the aluminum. **(a)** Bridged CPW resonator (extending to the right) coupled via a coplanar coupler to a bridged CPW feed line (vertical). **(b)** Vacuum-gap microstrip resonator (extending to the right) coupled via a parallel-plate coupler to a bridged CPW feed line (vertical).

4.2.5 Sacrificial Resist Removal

After the etching through the ground plane, the sacrificial resist is finally accessible through the newly created holes on top of the tunnel lines, at the wire bonding connection pads, and at the CPW feed lines and resonators. To remove the sacrificial resist from the vacuum-gap microstrips as well as from the air-bridges across the CPW segments and the parallel-plate couplers, we use an O_2 plasma (see fig. 4.6d). We choose a high pressure (10 Pa) for the oxygen plasma to make the etching more isotropic. That way the plasma is able to reach into the tunnels. However, as the resist has to be removed along the length of the tunnels and not as a thin film top-down, the etching time here is much longer than in usual plasma etching applications. The sample is kept in the plasma for 6 h or 12 h respectively (see section 4.3.6).

The finished sample is shown in fig. 4.8. While some corrosion damage can be observed at the edges of the created holes in the ground plane, the free-standing structures, i.e. the tunnels, bridges, and parallel-plate couplers remain intact.

4.3 Challenges

This section will elaborate on the problems and challenges encountered during the development of the described fabrication process as well as on the solutions and techniques deployed to overcome them. The topics discussed were not included in the description of the fabrication process to keep it concise. However, they will show the reasoning behind some decisions made during the development of this fabrication process, that are well suited to give insight into cleanroom development issues linked to such a complex process. Readers new to the topic might get an idea of what to expect, while readers well familiar with cleanroom development might find ideas and inspiration to adapt
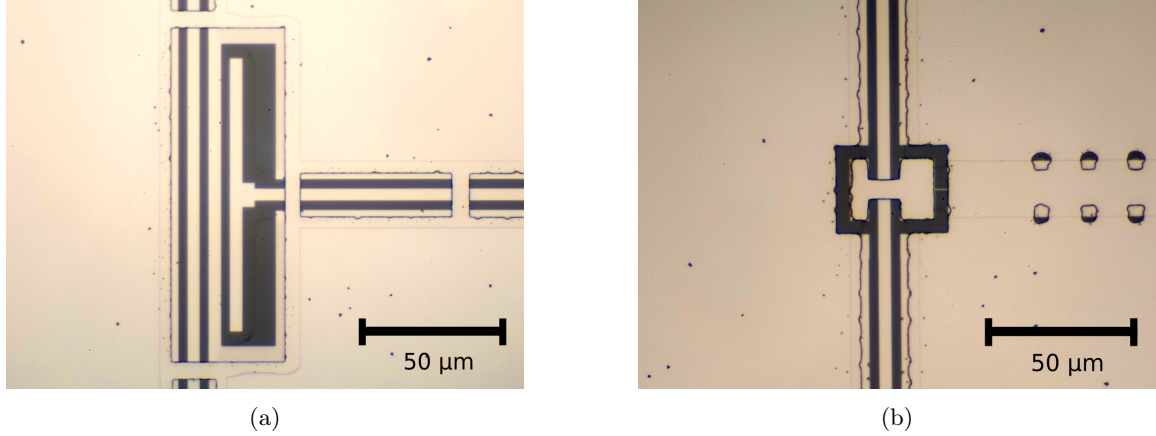
(a) (b)

Figure 4.8: Microscope images of the finished sample after the etching of the ground plane and the sacrificial resist. Aluminum appears bright, the silicon substrate dark gray. Some etching defects are visible at the edges of the aluminum and also on the ground plane. **(a)** Bridged CPW resonator (extending to the right) coupled via a coplanar coupler to a bridged CPW feed line (vertical). **(b)** Vacuum-gap microstrip resonator (extending to the right) coupled via a parallel-plate coupler to a bridged CPW feed line (vertical).

for their own problems and challenges.

4.3.1 Alignment and Drift

An important issue for every multi-layer process is alignment between the layers. A usual way to ensure this is to place reference marks on the wafer that can be utilized to correctly set the coordinate system for every lithography step. The alignment marks used for reference are crosses patterned in niobium with an MMA-PMMA bi-layer lift-off process. They are patterned on the wafer before the start of the vacuum-gap microstrip fabrication process as described above. Niobium is chosen because of its good visibility in the scanning electron microscope (SEM). Because of its high atomic mass and thereby interaction cross-section with electrons compared to aluminum, it remains visible in the SEM even through a few hundred nm of deposited metal.
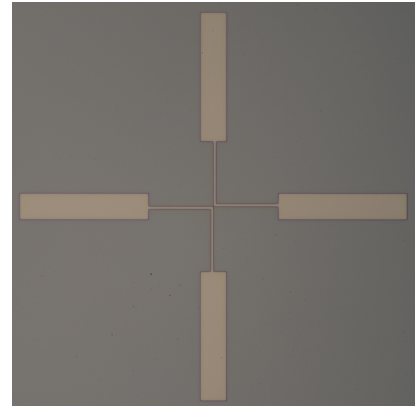
Figure 4.9: Niobium crosses are used for alignment between layers and for drift compensation

In addition to giving a point of reference between different lithography layers, the alignment marks can also be used to correct for drifts of the e-beam writer during the exposure by periodically checking their positions. In our case, thermal drifts were especially problematic, as the exposures of all three main layers (central structures, sacrificial resist, holes in the ground plane) are taking multiple hours. The measures taken against this issue were thermalization time before exposures and more importantly the already mentioned automatic drift compensation. With these actions, thermal drifts could be reduced to a few hundred nanometres largely independent of the exposure times. As the layout of the chip was designed with sufficient overlaps and tolerances to cope with

misalignment between layers of the order of approximately $1\,\mu m$, this is enough to ensure reliable results.

To obtain smooth and continuous lines for the central conductors of the resonators, the CPW elements, and the sacrificial resist lines, all long lines were patterned in "Fixed Beam Moving Stage" (FBMS) mode. In this mode, the electron-beam remains stationary while the stage, that the sample is clamped on, moves. This is in contrast to the usual deflection patterning mode, in which the whole area which should be written is divided into write fields. The e-beam writer then exposes one write field after the other using deflection of the electron-beam for patterning within that field. When one field is finished, the stage and thereby the sample is moved by one write field. This sometimes leads to problems for structures that extend over one or more boundaries between write fields and have therefore to be "stitched" together. The FBMS mode is a possibility to avoid those stitching problems.

4.3.2 Sacrificial Resist Deployment

When the sacrificial resist lines were first patterned on top of the thin central conductor lines of the tunnel resonators, they did not stick to the silicon after development. The use of an adhesion promoter (AR 300-80 from *Allresist*) was unsuccessful. Finally, to guarantee sufficient adhesion, the previous fabrication step was modified to include parallel metal stripes on both sides of the tunnel resonators. Fig. 4.10 shows an optical dark field image of the sample after the development of the sacrificial resist layer. For the vacuum-gap microstrip resonator (right part of the picture), the resist overlaps with the metal stripes on both sides of the narrow central conductor. We note that, although the central conductor with the two metal strips on each side looks similar to a CPW at this step, the two stripes will have very little effect on the capacitance of the transmission line. This is due to the much smaller separation of the central conductor from the ground plane above it, compared to the distances to the metal stripes on each side. Nevertheless, care has to be taken to ensure that the metal stripes included for resist adhesion are only partly covered by the resist lines. Should they be covered entirely they would in the end be disconnected from the ground plane and form resonators themselves.
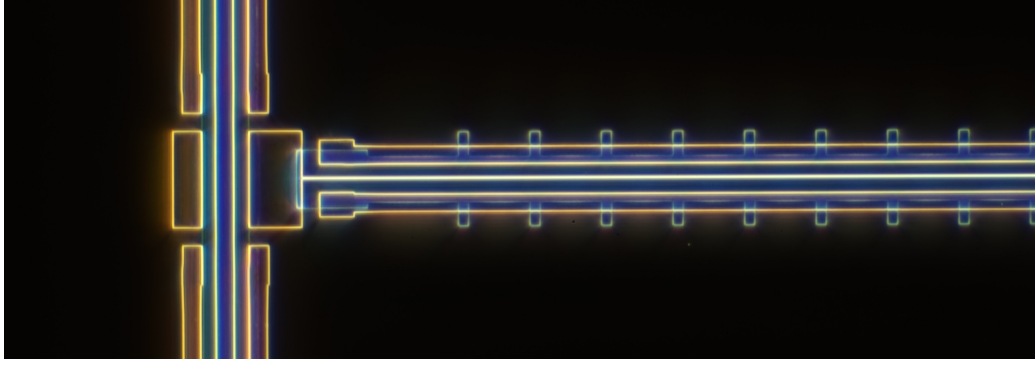
Figure 4.10: Optical dark field image after the deposition of the sacrificial resist. The image shows the same area on the chip as fig 4.5b. In this dark field image the aluminum structures show yellow edges, while the resist exhibits light blue edges. One can easily observe the overlap of the resist line with the underlying aluminum stripes and the characteristic smaller structures orthogonal to the main resist line covering the resonator.

4.3.3 Ground Plane Deposition

The deposition of the ground plane is subject to a number of requirements and restrictions to guarantee successful further fabrication and advantageous properties of the finished sample. We decide for a triple-layer structure made up by 10 nm of aluminum (deposited at 30° for improved step coverage), followed by 200 nm of niobium making up the main part of the ground plane, and finally terminated by a 50 nm layer of aluminum. The advantages offered by this design are:

Figure 4.11: Triple-layer structure of the ground plane.

- Selective etching of the 50 nm aluminum mask and the niobium layer is available, as CF_4 etches niobium much faster than aluminum. This is the reason why the aluminum hard mask works for the etching of the niobium layer.

- Superconductivity of all used materials ensures low dissipation in the ground plane

- The thin aluminum layer at the bottom of the structure acts as an etch stop for the CF_4 etch that else could attack the silicon substrate.

- Reactions between the sacrificial resist and the sputtered niobium are avoided by the thin evaporated aluminum layer.

- The presence of the thin aluminum film on the inside of the tunnels prevents the formation of unwanted niobium oxides, suspected to be accountable for significant portions of losses in microwave components [73–75].

- As a bonus the aluminum on top of the ground plane makes wire bonding to it easier, as

parameters do only need to be optimized for one target material (connection pads and top of ground plane both made of aluminum)

As listed above the thin bottom layer even serves a triple purpose. However, it comes with the drawback that, once it is reached with the CF_4 etch, special care has to be taken to remove it. Again deploying chlorine plasma would lead to more corrosion of the aluminum on top of the ground plane, as, at this step of the process, the resist mask does not protect it anymore. Also, it might pose a threat to the basic conductor layer that is protected only by the sacrificial resist at this point. For these reasons, we decided to mill through the thin aluminum layer at the bottom of the ground plane with an argon plasma that sputters the aluminum atoms by momentum transfer.

After this triple layer proved to be a viable solution to create holes in the ground plane, another problem became apparent. The ground plane is mostly made up by niobium, that, at the point at which the problem appeared, was still deposited by evaporation. Due to the high temperature of the material during deposition (see 4.1.1), the resulting film showed strong tensile strain, repeatedly destroying the constructed tunnels. To resolve this problem, a process to sputter niobium instead of evaporating it was developed. Sputtering allows for a higher level of control over the film parameters. A series of tests with niobium deposition on Kapton stripes resulted in a set of sputtering parameters for which the deposited niobium film showed vanishing tension. Kapton is suited well for these tests because of its flexibility that also shows low amounts of strain with curvature of the stripes.

4.3.4 Hole Etching

An essential part of the fabrication process developed is the creation of the holes in the ground plane to access the sacrificial resist. As described above, the solution of choice is a multi-step dry etching process.

To find working parameters and ensure reliable results under possibly slightly varying conditions, it is favorable to have a method to determine the progress of the current etching step in situ without having to take the sample out and examine it. The inductively coupled plasma (ICP) etching apparatus used is equipped with a camera and a laser aimed at the sample from the top of the chamber. The reflected intensity of the laser is measured, providing information about the surface reflectivity and thereby about the material properties. This allows for example to observe the change in the interference pattern of the laser reflected from a resist layer while the resist layer is progressively etched away. But also when etching into metal, the laser reflection brightness carries information about the material that is currently at the surface. For each etching step described in section 4.2.4, we observe a characteristic brightness curve telling us when the next layer is reached. As an example fig. 4.12 shows the curve that is observed when etching the topmost aluminum layer with the BCl_3 plasma. While for most of the etching time the intensity of the reflected laser beam does not change significantly, it decreases towards the end when the underlying niobium is reached. At the lowest point, when the curve is almost flat again the etching is finished for the examined
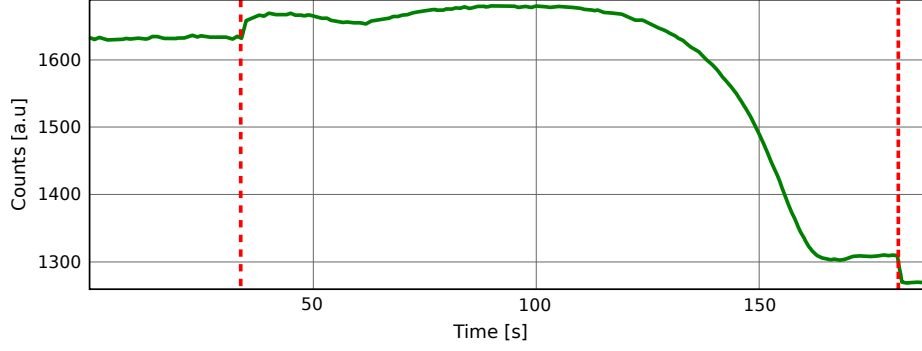
Figure 4.12: Laser reflection intensity measurement during BCl$_3$ plasma etching of the topmost aluminum layer. The vertical dashed lines indicate the ignition and extinction of the plasma.

spot, nevertheless, the plasma is kept on for an overetch of here 15 s.

4.3.5 Dicing

Dicing a wafer into individual chips is often a critical point in a fabrication process. To avoid damage done to the sample during dicing, it is helpful to spin a layer of protective resist on top of the wafer beforehand so that any particles that impact the surface of the chip can afterward be easily removed. This, however, forces us to do the dicing before the completion of the hole etching process. Any deposition of a liquid on top of the completely emptied tunnels poses the threat to destroy them by capillary action.

Therefore, the etching of the ground plane is interrupted after the BCl$_3$ etch of the first aluminum layer and the CF$_4$ conversion step. The wafer is covered by a layer of protective MMA resist. To guarantee accurate chip dimensions we use a laser cutter for dicing. This is necessary to ensure tight fitting into the PCB and to minimize the length of the wire bonds needed to connect the sample. As those are badly matched in terms of impedance they would degrade the microwave properties of the sample. The risk of breaking the chips while dicing is minimized by gluing (*Crystalbond 555HMP*) the sample to a copper stencil with pre-cut gaps where the wafer is to be cut. The dicing is done in two consecutive steps with different stencils to make cuts all around the individual chips. After each dicing step, the wafer is removed from the copper stencil in warm water, as the glue used is soluble in water and melting at a temperature of 66°. With that procedure, the individual chips can be separated from each other and from the rest of the wafer.

What could however be concluded after the fabrication and characterization of the sample discussed in this thesis, is that the process of removing the sample from the copper piece in hot water is responsible for at least some of the observed defects at the surface of the ground plane (see fig. 4.8). We suspect that the copper of the stencils and the *Crystalbond* glue in combination with the hot water bath leads to additional corrosion of the outer aluminum layer of the ground plane, or that the *Crystalbond* glue reacts with the protective resist and forms particles. Reactions of *Crystalbond* with resist and the resulting formation of particles were also observed in [76]. We suspect that a similar process might be responsible for the observed defects, however, no definitive conclusion on
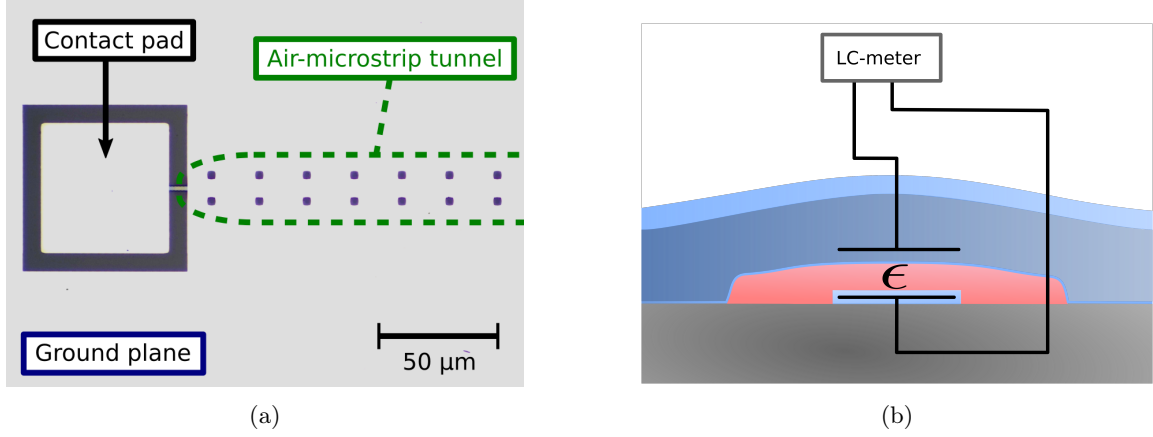
39

Figure 4.13: To obtain information about the status of the removal of the sacrificial resist from the tunnels, dedicated test structures were fabricated and measured with an LC-meter. **(a)** Optical microscope image of a capacitance measurement test structure. Aluminum appears bright, the silicon substrate gray and the holes on top of the vacuum-gap microstrip line appear blue. The microstrip extends far further to the right than is shown in this picture. **(b)** Sketch of a cut through a vacuum-gap microstrip transmission line. The capacitance measured is the capacitance between the central line and the ground plane. This capacitance is depending on the dielectric constant ϵ of the material in the tunnel.

this topic could be reached yet.

4.3.6   O2 Etching

For the success of the fabrication process, i.e. the significant reduction of the dielectric losses compared to a conventional microstrip, it is essential to remove the sacrificial resist from the tunnel cavities. However, it is hard to determine when all the resist is removed from the tunnels, as optical or SEM examinations are not suited to give information whether the resist is already completely removed.

One property that might provide insight in whether the O_2 etching of the resist is complete could be the capacitance between the central line and the ground plane. As the resist possesses a relative permittivity different from 1, we expect the capacitance to decrease when the resist is removed from the tunnels. In one of the earlier test structures we tried to use this to get an estimate for the time it takes the O_2 plasma to remove the resist completely. For this reason, room temperature measurements were done on test structures that were a few mm long straight tunnels with connection pads on both ends as shown in fig. 4.13a. The capacitance between the central conductor of the test structures and the ground plane on top (see fig. 4.13b) can be measured by contacting the contact pad with a small needle and the ground plane with another one. The two measurement needles were connected to an LC-meter, able to test the capacitance between the two contacts via driving and measuring RF-oscillations.

The capacitance between the central lines of the vacuum-gap microstrips and the ground plane was measured repeatedly while after each measurement the sample chip was exposed to the O_2 plasma. The time steps chosen were of 1 h length. Naive expectations were that the capacitance between
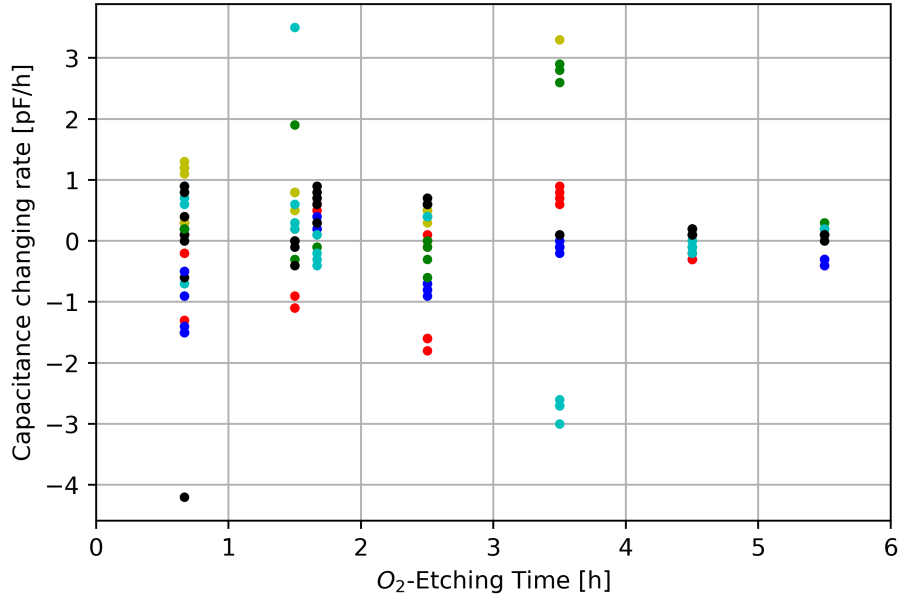
Figure 4.14: Mean capacitance change caused by one hour of additional O_2 etching. The x-axis is showing the O_2 etching time up to the measurement point. Different colors correspond to to slightly different tunnel designs.

the central lines and the ground plane would monotonously decrease while etching and converge to a final value when all the resist is removed.

The measurement results, which are presented in fig. 4.14 show, that the processes involved are more complicated than expected. The difference in capacitance gives us a mean rate of change for the time the sample was etched. In the plot, this rate is then attributed to the mean point in time between the two measurements. That means, that if a particular line was measured after 3 h of O_2 etching and then again after 4 h, the corresponding difference would be plotted at 3.5 h. Different colors in the figure correspond to slightly different tunnel designs.

We observe almost random increases and decreases in capacitance without any apparent pattern. The fact that the capacitance also sometimes increases when resist is removed, leads us to the conclusion that when the resist is removed, stress in the ground plane is released, leading to the tunnel roof moving closer to the central conductor. These measurements were taken at an early point of the development of the vacuum-gap microstrip, where the ground plane was still deposited using evaporation. Therefore, the information that we get from this measurement for the current sample is limited. However, the fact that the capacitance is still changing after 3 h of O_2 etching implies that the resist at this point is not completely removed yet. Changes in both directions become smaller after approximately 4 h, hinting that at that point in time the resist could be mostly removed from the tunnels. The etching time of 6 h or 12 h respectively is chosen with this information in mind.

4.4 Room for Improvement

After discussing the fabrication details of the vacuum-gap microstrip resonators treated in this thesis, it is worthwhile to point out in which aspects the current process can still be improved and how current limitations on performance and characterization can be overcome.

An issue still remaining with the sample presented in this thesis are the defects on the outer surface of the ground plane, as visible in fig. 4.8. As the copper stencil and the glue with which the sample is glued on are one of the suspected causes for this problem, it will be worthwhile to experiment with replacements for either or both of them. Also reducing the temperature during the dissolving of the $Crystalbond^{TM}$ glue and the detachment of the wafer from the support might help. The resolving of this issue could improve the transmission properties of the CPW feed line and maybe also the performance of the vacuum-gap microstrip resonators.

Another path that is already being investigated is realizing the aluminum mask creation as a lift-off process rather than as a resist masked etching process. This promises more accurate and clean hole edges and more stable parameters working for both, large and small structures. To achieve this, one has to optimize a bi-layer lift-off process with a sufficient undercut using a negative resist.

To optimize the O_2 etching time for removal of the sacrificial resist, further investigations are required. Those could be done either by fabricating several samples, exposing them to different amounts of O_2 etching time and comparing their internal quality factors or by going back to the fabrication of dedicated test samples that can be analyzed with different techniques. What again appears worthwhile are capacitance measurements using an LC-meter as the tensile strain that influenced this analysis at an earlier stage has been reduced with changing the ground plane deposition method to sputtering. Another option to put a boundary on the amount of sacrificial resist left in the tunnels is X-ray photoelectron spectroscopy (XPS) in combination with simultaneous argon beam milling. After breaking through the ground plane with the argon milling, the signal of the carbon contained in the resist will allow conclusions to which degree the resist is removed from the tunnels. To make this measurement meaningful, high areal densities of vacuum-gap microstrip tunnels are required because of the comparably large argon beam size and the rather low sensitivity of this method towards carbon.

Chapter 5

Sample Design and Experimental Setup

The purpose of the samples fabricated and analyzed in this thesis is to test and demonstrate the performance of vacuum-gap microstrips and air-bridges fabricated with the newly developed fabrication process described before. Of most importance for the intended use of the vacuum-gap microstrip, namely for the use in TWPAs, are its losses. To test the losses, resonators are built from the transmission lines.

This chapter leads the reader through the design of the sample and the experimental apparatus used to measure it at cryogenic temperatures. First, the design of the resonators will be presented by explaining the implementation of vacuum-gap microstrip and bridged CPW transmission lines using our fabrication process. Afterward, the coupling of these resonators to a feed line with different capacitive coupler designs will be discussed. The mounting in a sample holder finally allows for measurement in a dilution refrigerator, using standard microwave measurement techniques.

5.1   Transmission Line Design

Transmission lines are arguably the most basic component of microwave circuits. The fabrication process that was described in the previous chapter enables us to design transmission lines in two different geometries, vacuum-gap microstrips and bridged CPWs (see section 3.1.1). These two geometries allow to access different impedances, which is very useful experimentally. Moreover, the different geometries make it possible to investigate the origin of appearing losses, thanks to their very different electrical field pattern. Those transmission line designs are used in the investigated samples to form feed lines and distributed quarter wave resonators.

5.1.1 Vacuum-Gap microstrip Transmission Line

The basic working principle of the vacuum-gap microstrip transmission lines is based on the thin vacuum gap separating the central conductor from the ground plane above it. Due to the close distance, the transmission line shows high capacitance per unit length. This distance is fixed by the sacrificial resist thickness. To match the transmission line to the usual $50\,\Omega$ of characteristic impedance, we choose a central conductor design width of $150\,\mathrm{nm}$, according to a 2.5D electromagnetic simulation tool. At the time of the design of the sample, the height of the tunnels was estimated to $80\,\mathrm{nm}$ based on height measurements of the thickness of the resist on the unpatterned surface of a wafer. Both those values can differ slightly because of the local patterning of the wafer. Determining exact values is feasible only after finishing the sample (see section 6.1).

In terms of layer design, a vacuum-gap microstrip is made up by the central conductor and the adhesion promoting metal stripes (see section 4.3.2) on the basic layer. It is continued with the sacrificial resist lines on top of the conductors of the base layer. The last design layer contains the holes that are placed in the ground plane to access the sacrificial resist. The drawing of these three layers forming a vacuum-gap microstrip is shown in fig. 5.1a. The $150\,\mathrm{nm}$ wide central conductor is placed in the $6\,\mu\mathrm{m}$ wide gap between the two broad metal stripes to ensure sufficient separation for possible misalignment between the layers. The width of the sacrificial resist line is designed to be $8\,\mu\mathrm{m}$ to entirely cover the gap and have some overlap with the adhesion promoting stripes at the sides. Also, the overexposure of the resist lines, which was done to form smoother edge profiles of the tunnels, leads to the resist line being around $2\,\mu\mathrm{m}$ wider than designed, increasing the overlap with the adhesion promoting stripes. The continuous, wide sacrificial resist line is modified by periodic smaller extensions on both sides. The holes, used to access the resist afterward, are placed on top of these extensions, to have a sufficiently large distance between them and the central conductor. This distance is needed to avoid any possible negative influence that the ground plane etching process or the presence of the holes might have on the microwave performance of the transmission line.

5.1.2 Bridged CPW Transmission Line

As a side result, the fabrication process of the vacuum-gap microstrip can also be used to create air-bridges. Those are often used for ground plane connection when the ground plane is interrupted by gaps as they appear for example in CPW transmission lines. If proper connection between separated parts of a ground plane is not ensured, parasitic slot line modes can appear [77].

Air-bridges can be produced manually by wire bonding between the different sections of the ground plane [34, 41] or by means of micro-fabrication. When air-bridges are fabricated on chip, their height and thereby their separation from the CPW central conductor is usually in the order of micro meters [78–80]. For wire bonds, these distances are even larger. As the process of the vacuum-gap microstrips was developed with a gap of approximately $80\,\mathrm{nm}$ to provide high capacitance, the air-bridges that are created by this method are much closer to the central conductor of the
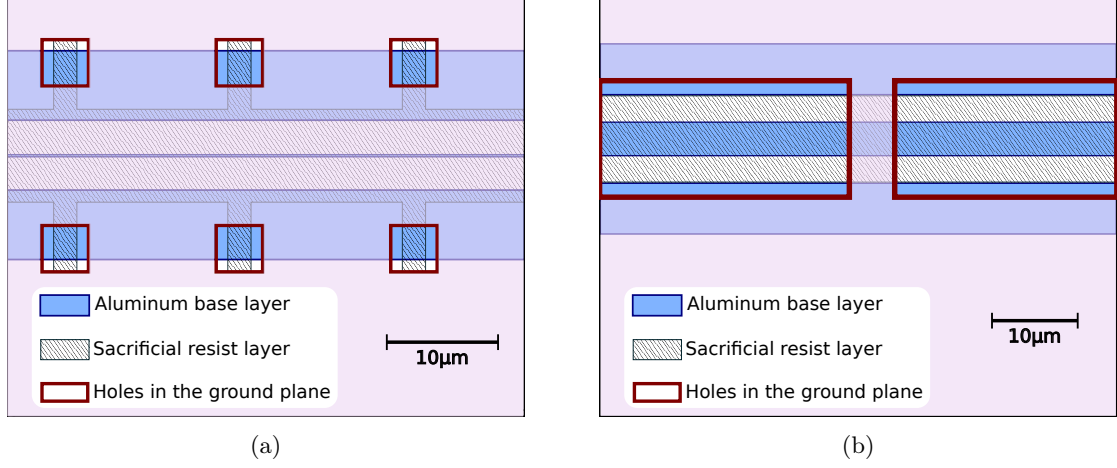
Figure 5.1: On the investigated sample, transmission lines are realized in vacuum-gap microstrip and bridged CPW design. The sketches show how the three design layers are combined to form them. **(a)** Vacuum-gap microstrip. **(b)** Bridged coplanar waveguide.

CPW. Therefore, it is important to take their additional capacitance into account when designing transmission lines.

To obtain a characteristic impedance of the transmission line of $50\,\Omega$ we start by a classic CPW with an impedance higher than $50\,\Omega$ and then reduce it by including short tunnel segments acting as air-bridges and effectively reducing the characteristic impedance of the line. Using *Sonnet* simulation data of the bridged and unbridged segments and assuming simple linear combination of their impedance values, we obtain the ideal fraction of the CPW that should be covered by air-bridges. To avoid problems with the fabrication, we conservatively choose a width of $5\,\mu m$ for the bridges, which results in a bridge interval of $55\,\mu m$.

Here it is worth mentioning, that the high capacitance bridge sections and lower capacitance unbridged CPW sections form a periodic pattern which could create nonlinear dispersion and even stopbands for signals traveling along those lines. However, wavelengths comparable to the bridge intervals are achieved only by signals with frequencies far above the intended measurement range of approximately $4\,GHz$ to $12\,GHz$. To achieve for example $\frac{\lambda}{4} = 55\,\mu m$, more than $500\,GHz$ are necessary.

Figure 5.1b shows a sketch of a bridged CPW. Again it is made out of the fabrication layers that were already introduced before, namely the aluminum base layer, sacrificial resist layer, and ground plane holes layer. Because of the lower capacitance that can be obtained in this geometry, the central conductor of the CPW is much wider than the central conductor of the vacuum-gap microstrip, resulting in reduced inductance. The gap between the central conductor and the ground plane is $3\,\mu m$ on each side.

To cover the whole CPW, the width of the sacrificial resist line is chosen to be $10\,\mu m$. Because of the overexposure increasing the width in the end, still sufficient overlap with the return conductors to provide good adhesion is present. Although the overlap of the resist with the return conductors
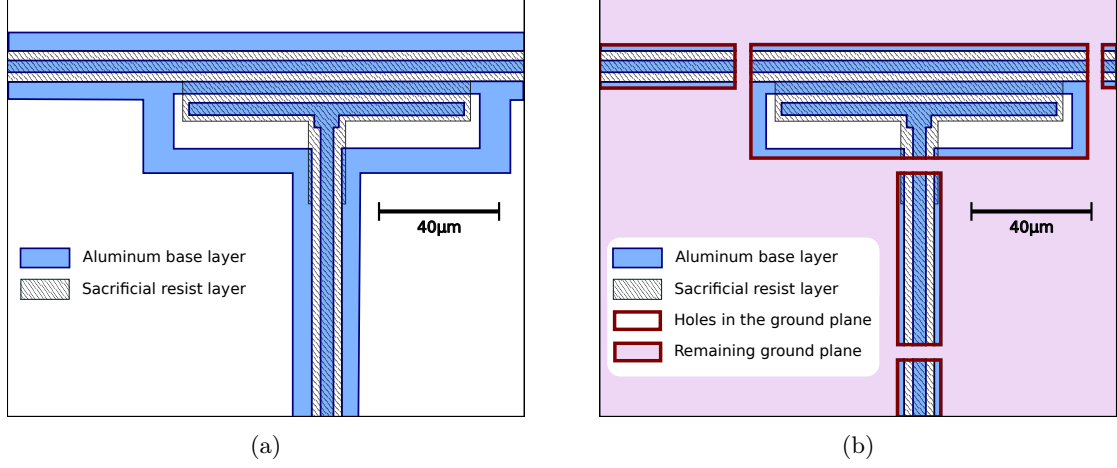
Figure 5.2: For weak coupling between the resonators and the feed line, coplanar capacitive couplers are sufficient. Here a bridged CPW resonator (extending to the bottom) is coupled capacitively to a bridged CPW feed line (horizontal) via a coplanar metal strip. For better visibility, the sketch from **(a)** shows only the first two layers while **(b)** also includes the ground plane with the etched holes.

of the CPW is important for the adhesion of the resist, it is also essential that the resist does not entirely cover them. In this case, the return conductors would not be well connected to the ground plane that is deposited afterwards, potentially leading to parasitic modes, as the separated return conductors act as resonators.

As the final layer, the design for the CPW transmission lines includes rectangular holes of $50\,\mu m \times 14\,\mu m$, where the ground plane is removed from the top of the CPW lines. In the $5\,\mu m$ long gaps between the rectangular patches, the ground plane remains and forms bridges. When the sacrificial resist is removed, the air-bridges are released as free-standing structures over the CPW.

5.2 Capacitive Couplers

To measure the resonators made from these transmission line designs, they need to be coupled to a feed line, which is done with capacitive couplers. Different capacitances and thereby different coupling quality factors were implemented, as the internal quality factor for the finished resonators is yet to be determined. To obtain reliable results for the circle fit (see section 3.1.4), the coupling quality factor Q_c should be similar to the internal quality factor Q_i. We chose to implement couplings, that result in the coupling quality factors $Q_c \in [10,^3, 10^4, 10^5, 10^6]$. For the weak couplings, i.e. low capacitances, it is sufficient to design coplanar coupling capacitors, but for achieving strong coupling, coplanar couplers would become large and unpractical. Therefore, we use the newly acquired method of building tunnels and bridges to design couplers in parallel-plate geometry. It is worth noting, that both coupler designs can be applied to both resonator geometries.
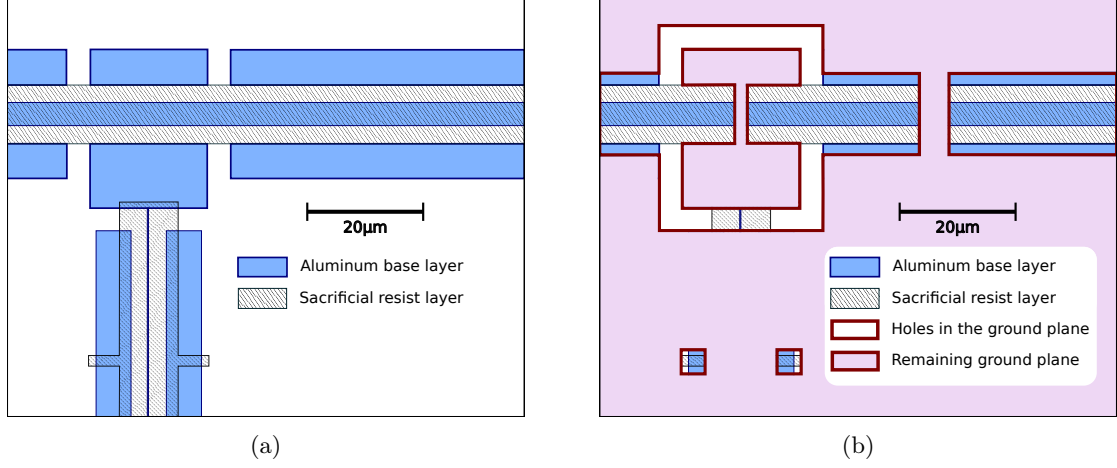
Figure 5.3: To achieve strong coupling between the resonators and the feed line, parallel-plate couplers in a bridge design are used. Here a vacuum-gap microstrip resonator (extending to the bottom) is coupled capacitively to a CPW feed line (horizontal) via an air-bridge. For better visibility, the sketch from **(a)** shows only the first two layers while **(b)** also includes the ground plane with the etched holes.

5.2.1   Coplanar Coupler

Figure 5.2 shows how coplanar couplers are implemented in our sample. The central conductor of the resonator is terminated in a metal strip parallel to the feed line. By varying the length of the strip, one can change the coupling capacitance between the resonator and the feed line. The coplanar coupler is protected by a layer of sacrificial resist and opened up by a large rectangular hole on top. Because of the resulting large gap in the ground plane, air-bridges are included directly beside the coupling structure to reduce the parasitic inductance created by the hole.

5.2.2   Parallel-Plate Coupler

For obtaining strong coupling between the resonators and the feed line, large capacitance values are needed. We therefore use the newly developed fabrication process to build vacuum-gap parallel-plate couplers. Those couplers are designed like the bridges over the CPW feed line discussed above, but in contrast to those are disconnected from the ground plane and connected to the central conductor of a resonator.

Figure 5.3 shows a drawing of the three design layers a parallel-plate coupler consists of. The central conductor of the resonator, be it a vacuum-gap microstrip or CPW resonator, is connected to a metal pad beside the feed line. An air-bridge, as already described above, spans from that pad to a piece of metal on the other side of the CPW. The hole in the ground plane, which is patterned around the coupling bridge, separates the bridge and the connected pads from the ground plane around it.

The capacitance between the bridge and the central conductor of the feed line is dominating over the parasitic capacitance between the metal pad and the feed line because of the small separation. Like for the coplanar couplers the specific coupling strength can be designed by varying the length
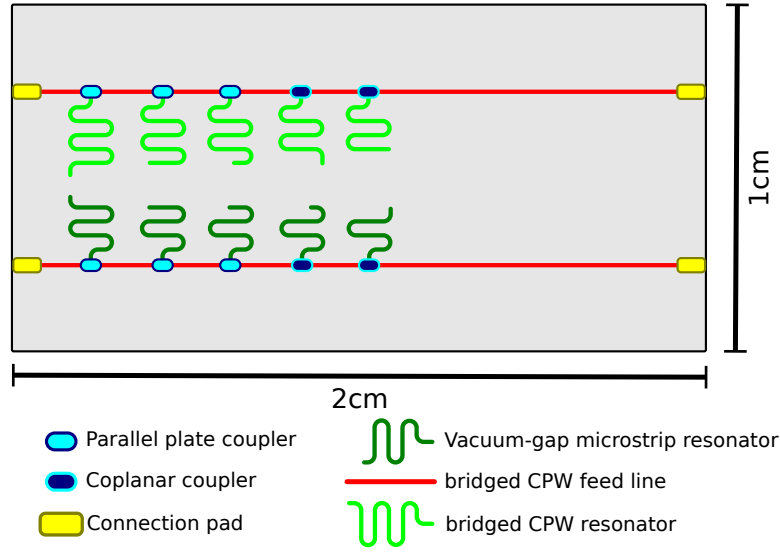
Figure 5.4: Schematic of the sample chip layout. Each feed line is terminated by connection pads and contains 5 resonators in either vacuum-gap microstrip (dark green) or bridged CPW (light green) design. These resonators are coupled to the feed lines using parallel-plate and coplanar couplers of different coupling strengths.

of the structure, however, the necessary length is significantly smaller for a given capacitance. From electromagnetic simulations a parallel-plate capacitor of $2\,\mu m$ is approximately equivalent to a $90\,\mu m$ coplanar coupler. Both show a capacitance of approximately $1.4\,fF$. These numbers were obtained by simulation for a frequency of $9\,GHz$, a central conductor width of $4\,\mu m$ and an assumed tunnel height of $80\,nm$. As we will see later using scanning electron microscopy (SEM) and atomic force microscopy (AFM), the dimensions of the finished sample differ slightly from this design, resulting in even higher capacitance of the parallel-plate couplers.

5.3 Chip Layout

The dimensions of the designed chip are $2\,cm \times 1\,cm$, allowing to easily fit 3 chips on a 2-inch wafer. The basic chip layout is shown in fig. 5.4. Each of the chips contains two bridged CPW feed lines, each coupled to 5 resonators in the two different transmission line geometries described above, i.e. vacuum-gap microstrip and bridged CPW design. Each feed line is terminated on both ends by a connection pad for wire bonding. In addition to the components shown in the figure, each chip also contains test structures for different design parameters and a dedicated area for the laser reflection measurement, used to determine the end of the etching processes. Those extra structures are placed in the seemingly empty space on the right of the sample chip.

5.4 Measurement Setup

The fabricated chips are integrated into a cryogenic measurement setup for characterization. In this section, we will talk about the analyzed chips, show their mounting in a sample box and introduce the cryogenic setup and the instrumentation that was used for the measurements.

5.4.1 Investigated Devices

Using the layout as presented before, three chips were fabricated on one wafer, two of which were investigated in terms of their microwave properties. Two chips were necessary, because in the first chip that was cooled down (**Chip 2**) only the feed line containing the vacuum-gap microstrip resonators was intact, while the feed line containing the bridged CPW resonators was damaged. Therefore, after the analysis of **Chip 2** was completed **Chip 1** of the same wafer was investigated.

The main part of the fabrication process for the two chips is identical, the only part where they were treated separately is the etching of the ground plane that takes place after the wafer is diced into the individual chips. The processing of the chips differs in the time that they were exposed to O_2 plasma. **Chip 2** was left in the O_2 plasma for 6 h, **Chip 1** for 12 h. Also, **Chip 1** received a short dip in TMAH before the O_2 etching in order to remove some suspected aluminum residue.

What has to be noted for **Chip 1** is that because of the TMAH dip a number of defects were observed at the bridges and parallel-plate couplers. Those were observed to be partly lifted up, above their designed position. Still, their loss properties should be very similar to a fully functional device, making further analysis of the sample useful. However, the coupling capacitances are expected to significantly differ from the design values.
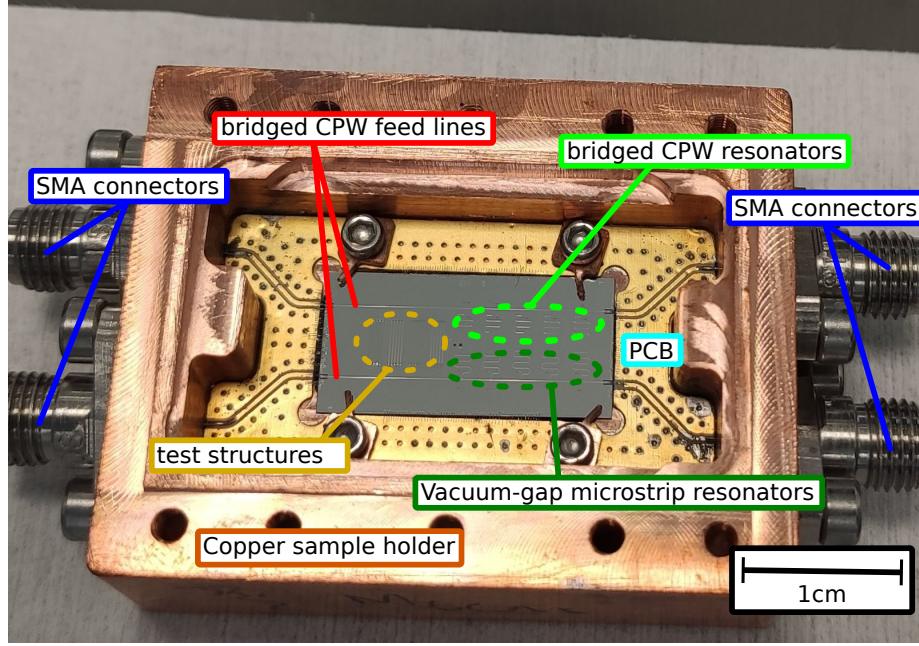
Figure 5.5: Photograph of the sample clamped to the copper sample box and wire bonded to a PCB. The PCB conductors are soldered to SMA connectors on the outside of the box.

5.4.2 Sample Holder

To connect the chip to the measurement setup, it was installed in a copper box with a printed circuit board (PCB). The chip is connected to the circuit board via wire bonding using $25\,\mu m$ aluminum wires. The wire bonds connect the central conductors of the PCB to the connection pads of the feed lines and the ground plane of the PCB to the ground plane of the chip. Standard SMA connectors soldered to the PCB then serve as the connection points to all further wiring. The copper sample holder was designed using the *Solidworks* CAD software and fabricated in the house-intern workshop. When designing the dimensions of the box, care was taken to place the electromagnetic resonances of the box outside the desired working range of our measurement setup. An image of the sample chip in the copper box is shown in fig. 5.5. The sample is clamped with four screws offering a simple way of exchanging it. What is not shown in this figure is the copper lid that was used to close the box.

5.4.3 Cryogenic Setup and Instrumentation

The sample holder is placed in a dilution refrigerator from *Oxford Instruments*. Figure 5.6 shows the measurement setup in the context of the different temperature stages of the refrigerator. The sample box is mounted at the base plate at a temperature of approximately 20 mK.

All microwave measurements presented in this thesis are taken with a vector network analyzer (VNA). When measuring transmission, the VNA emits well-defined frequencies through one of its ports and simultaneously measures the power incident on its second port. By sweeping the emitted frequency one obtains a transmission spectrum of the network in between the two ports. A modifiable digital step attenuator is placed after the VNA output, making large-range power variation possible. Three fixed attenuators at the different temperature stages of the fridge attenuate the input signal, suppressing thermal noise coming from the higher temperature stages. The sample box is connected to an RF-switch on the input as well as on the output side. This enables consecutive measurement of both feed lines through the same input and output lines. On the output side of

Figure 5.6: Schematic of the measurement setup. The output port of the VNA is connected via a series of attenuators at decreasing temperatures to the sample at 20 mK. A switch enables the investigation of both feed lines in one cool-down. On the output side the VNA signal passes through circulators, is amplified by a high electron mobility transistor (HEMT) and a room temperature amplifier, and is finally fed back to the second port of the VNA.

the setup, the sample is isolated from the following amplifiers by a series of three circulators (only one shown in the sketch). On the 4 K stage the signal gets amplified by a high electron mobility transistor (HEMT) followed by a room temperature amplifier before being fed back to the VNA. The input attenuation amounts to approximately 60 dB including also the loss introduced by elements like filters and cables not explicitly shown in fig. 5.6.
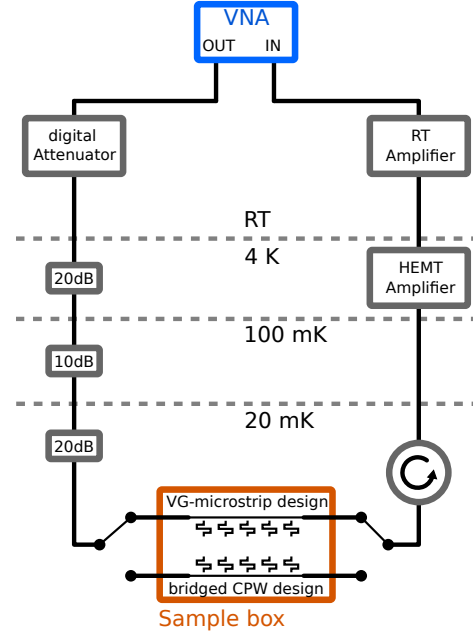
Chapter 6

Results and Discussion

This chapter is dedicated to the presentation and discussion of experimental results of two samples fabricated during this master thesis. First, optical, scanning electron, and atomic force microscopy will be used to infer properties of the surface structures as well as the vacuum-gap microstrip tunnels. Special focus is put on the AFM analysis, as the images produced by its data offer insightful new information about the properties of our sample, while at the same time giving an accessible and intuitive way to look at it. Subsequently, microwave measurements in a dilution refrigerator will be discussed, analyzed, and put into context. This includes the extraction of the quality factor of the fabricated resonators as well as the power and temperature dependence, which makes it possible to get an estimate for the kinetic inductance ratio (see section 3.2.2).

6.1 Imaging and Surface Analysis

Different methods were used to monitor the ongoing fabrication process as well as analyze the finished sample afterward. Optical microscopy is the easiest way to monitor the sample during fabrication. It was used to verify the correct patterning of the different layers and to spot problems in any fabrication step as soon as they appear. Some of the optical images taken at the different steps of the fabrication process are presented in chapter 4 along with the description of the process. For a more thorough analysis of the finished sample, however, optical microscopy is not sufficient. Therefore, we used scanning electron microscopy (SEM) to measure the final dimensions of the patterned structure along with atomic force microscopy to obtain information about the vertical dimensions of the sample.
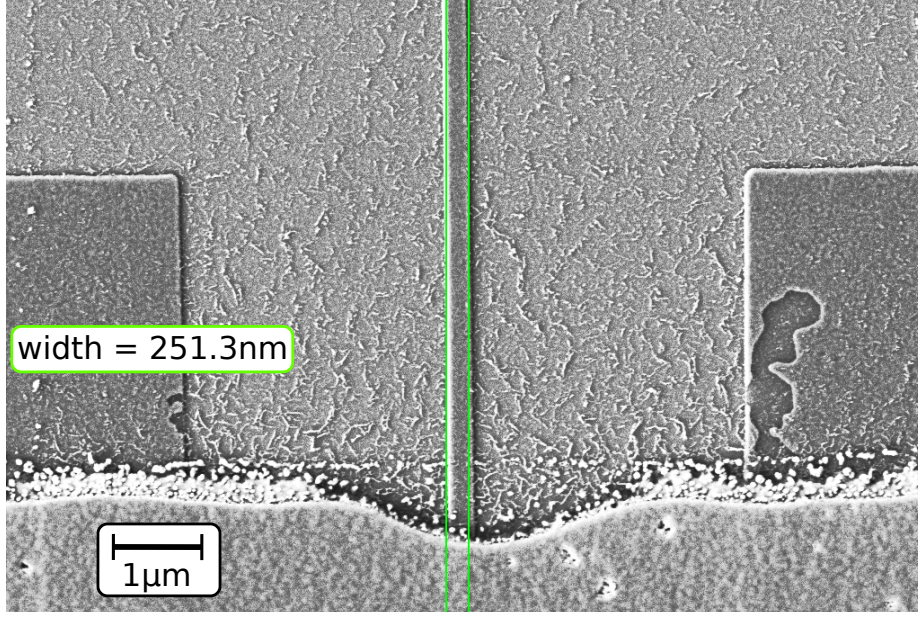
Figure 6.1: SEM image of the central conductor of a tunnel resonator. The green lines show that the final width is about 100 nm larger than the designed width. Defects that are visible in this image are the residue on the silicon substrate, the grainy structures along the tunnel edge, and the defect in the aluminum sticking stripe on the right.

6.1.1 Scanning Electron Microscopy (SEM)

While taking more time and effort than optical examination, SEM imaging offers the advantage of much better magnification. This can be used to measure the dimensions of the patterned structures as well as to get more information on fabrication defects that may remain hidden in optic images.

Dimension Analysis

Fig. 6.1 shows an SEM image of the central conductor of a resonator entering a tunnel structure. One can see that the narrow central line, designed to be 150 nm wide, is in reality wider than that. This is due to the high dose that was necessary to expose these narrow structures. Electrons get scattered from this high-dose area and also from the nearby large adhesion stripes (see section 4.3.2) to adjacent areas and lead to exposure of those. This is known as proximity effect. Also, it has to be mentioned, that creating such a narrow gap in a much thicker resist layer is challenging in its own right. In this context, a relevant number is the aspect ratio between the height and width of a patterned structure. In our case, the thickness of the resist layer is almost 1 μm, which would mean an aspect ratio of approximately 6:1 for the designed 150 nm. Especially for very narrow features (<1 μm) these effects will have to be taken into account for future designs.

Defects and Residue

In optical images, residue and defects that are smaller than the resolution of the microscope, ultimately given by the wavelength of the used light, remain invisible. SEM images can provide information about the microscopic cleanness of the sample. When looking at fig. 6.1 and fig. 6.2, three of the problems present in the current fabrication process become apparent.

First of all, the edges of the holes in the ground plane are not straight, but show indentations on a length scale of a few µm because of corrosion of the aluminum mask used for the creation of the holes (see section 4.3.5). The same effect is thought to be also responsible for the fine grains visible along the edges. Those particles are problematic because they might lead to partial or complete shorts of the transmission lines. Moreover, they can cause additional microwave loss because of their sharp topology.

Secondly, where the sacrificial resist was removed from the surface, residue is covering the sample. This residue is also visible on the AFM images from fig. 6.3 and fig. 6.4. We suspect that this residue is formed while breaking the last aluminum layer on top of the resist by argon milling (see section 4.3.4). During this step, the aluminum and the resist might react and form this residue, which is removed neither by the argon milling nor by the O_2 etching of the sacrificial resist. We do not expect this residue to affect the performance of the vacuum-gap microstrip resonators greatly, as the resist in the tunnels is not exposed to argon milling and should therefore not exhibit this behavior. The bridged CPW resonators, however, will be influenced more by this residue, as they are covered by it over almost their entire length.

The third issue visible is the defect on the right metal strip in fig. 6.1. This is likely caused by a particle or a small detached piece of resist covering that spot during metal deposition. In the position it is appearing here, namely in the ground plane, a defect like that is not a big problem. However, such defects can break a resonator or feed line, making the sample impossible to measure.

6.1.2 Atomic Force Microscopy (AFM)

To analyze the surface structure and extract further details on the final dimensions of our fabricated sample, an atomic force microscope (AFM) was used. We want to thank the group of Univ.-Prof. Dr. Martin Beyer and especially Simone Schirra for making this measurement possible. The AFM measurement was performed after the creation of the holes and a short O_2 cleaning step, but before the removal of the sacrificial resist from inside the tunnels. Two areas on the chip were imaged, a long coplanar coupler of a bridged CPW resonator (see fig. 6.3) and a parallel-plate coupler of a vacuum-gap microstrip resonator (see fig. 6.4). Optical microscope images of the same areas are shown in fig. 4.5.

An accessible way to present the height data from the AFM measurements is via 3D images. In those, the overall surface profile and also roughness and defects are very well visible. However, it is
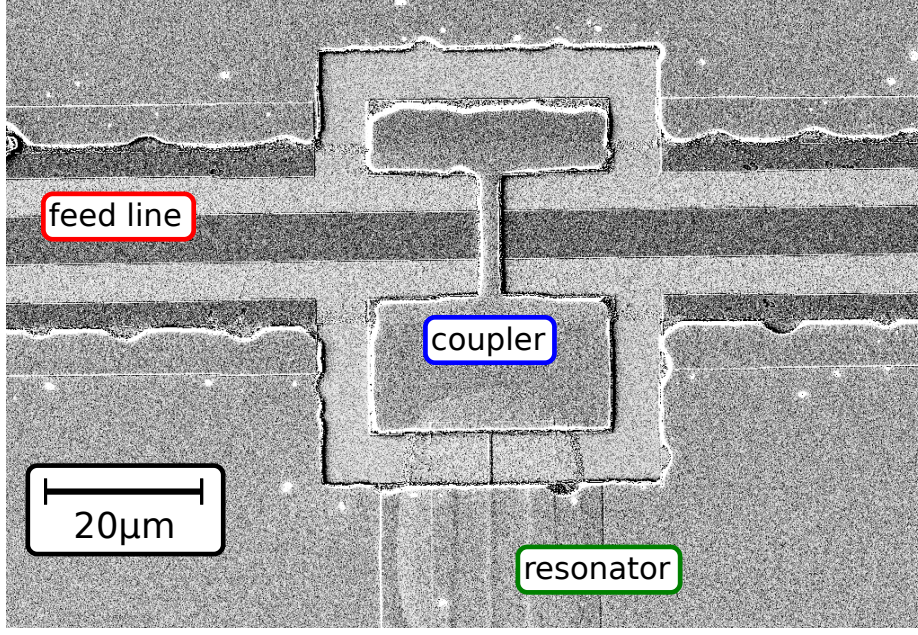
Figure 6.2: SEM image of a parallel-plate coupler. A vacuum-gap microstrip resonator (central conductor and start of the tunnel visible in the bottom of the picture) is coupled via a parallel-plate coupler to a CPW feed line (left to right).

important to note that the images presented show a largely exaggerated z-dimension of the samples. This is necessary to show the relevant features but gives a wrong impression of the overall very flat surface of the sample. The lateral dimensions of the discussed scans span up to $100\,\mu m$ while the maximal height difference observed is of the order of a few hundred nm.

In addition to the qualitative visualization, the AFM measurements were also used to quantitatively determine the vertical dimensions of the structures and the thickness of the deposited materials. The relative heights are obtained by direct comparison of height in neighboring regions. From these measurements, we obtain a value of $50(5)\,nm$ for the thickness of the basic aluminum layer, compared to the designed $40\,nm$. The ground plane has a thickness of $323(5)\,nm$. This is also more than the designed $260\,nm$ ($10\,nm$ of Al + $200\,nm$ of Nb + $50\,nm$ of Al). These results suggest imprecise calibration of the material deposition. The given uncertainties are estimated by repeating the measurement at different locations and comparing the results.

As already mentioned in the process description, the sacrificial resist film has a thickness of approximately $80\,nm$ on flat surfaces. This value is obtained by ellipsometric measurements. However, the local topology of the sample, i.e. the already deposited first layer does influence the resist thickness locally. This effect can not be neglected as the thickness of the aluminum and the sacrificial resist are comparable. Another factor that changes the thickness of the resist is the argon milling taking place before the ground plane deposition. To extract information about the tunnel height, we take an AFM measurement of a short section of a vacuum-gap microstrip resonator and extract the height profile as shown in fig. 6.5.

By assuming constant thickness of the ground plane over the imaged area, the changes in height

55
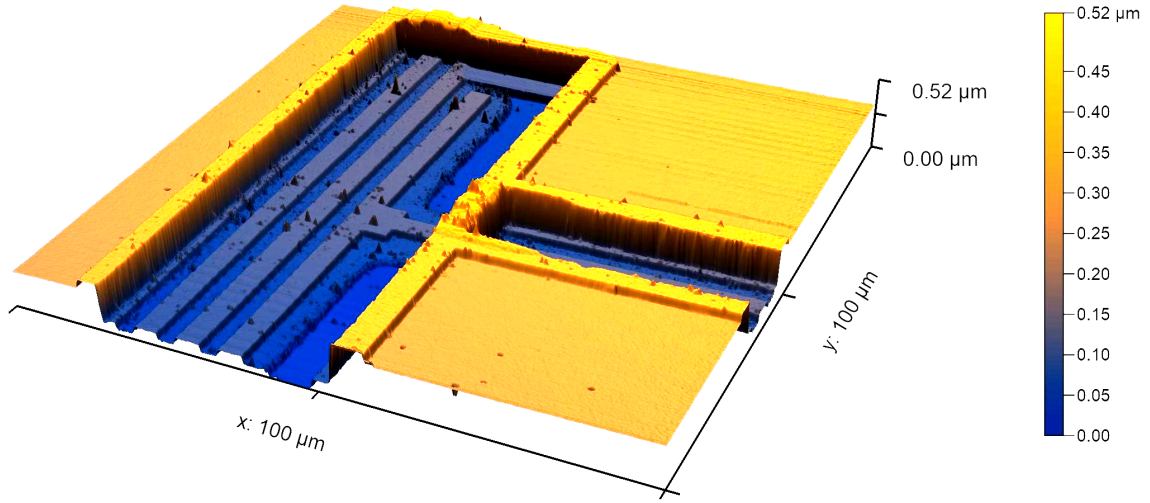
Figure 6.3: 3D representation of the AFM height data (z-axis and color) of a coplanar coupler. The coplanar coupling strip (T-shaped structure in the center of the image) couples a bridged CPW resonator (extending to the right) to the bridged CPW feed line (from the front to the back). Two air-bridges connecting the ground plane segments separated by the CPW structures are visible in the center and in the very back of the image. For reference, compare this image to the design sketch from fig. 5.2, and to the optical microscope image from fig. 4.8a.
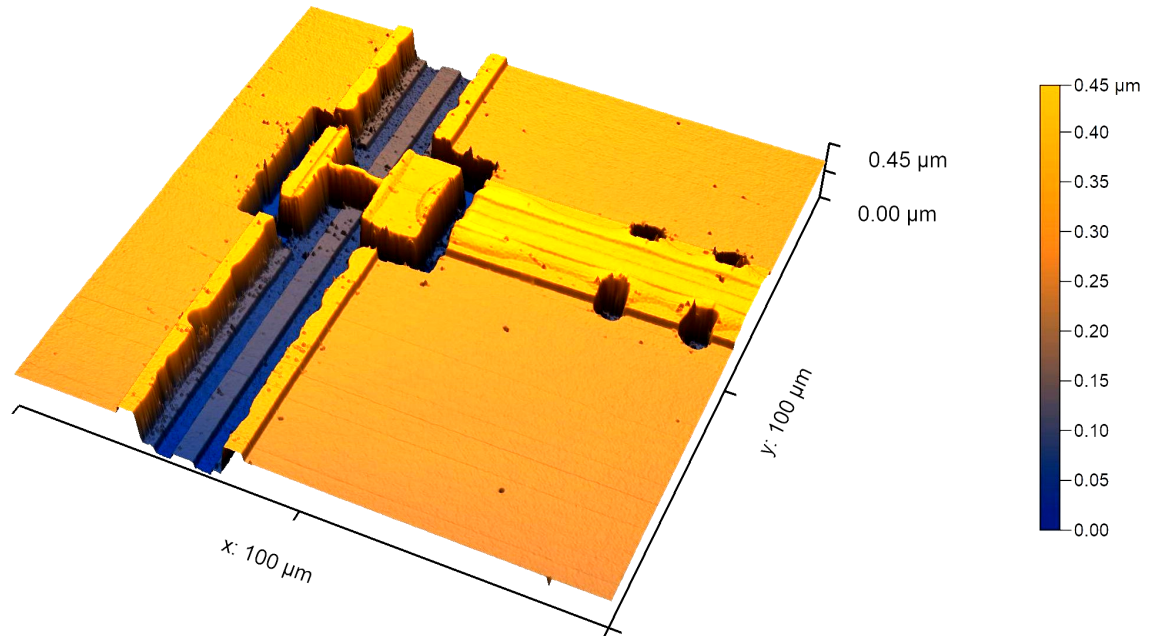
Figure 6.4: 3D representation of the AFM height data (z-axis and color) of a parallel-plate coupler. The coupling bridge (H-shaped structure in the center of the image) couples a vacuum-gap microstrip resonator (extending to the right) to the bridged CPW feed line (from the front to the back). Four holes in the ground plane used to access the sacrificial resist in the tunnel are visible in the right part of the image. For reference, compare this image to the design sketch from fig. 5.3, the SEM image from fig. 6.2, and the optical microscope image from fig. 4.8b.

Figure 6.5: The AFM height data can be used to extract information about the form and dimensions of the tunnels. The data analyzed here is a zoom on the vacuum-gap microstrip tunnel on the right of fig. 6.4. **(a)** AFM height scan of a vacuum-gap microstrip tunnel. The height data is given by the color. **(b)** AFM height data (green curve) across a vacuum-gap microstrip tunnel (data marked in red in (a)). The individual height contributions of sacrificial resist and aluminum conductors are shown in color.
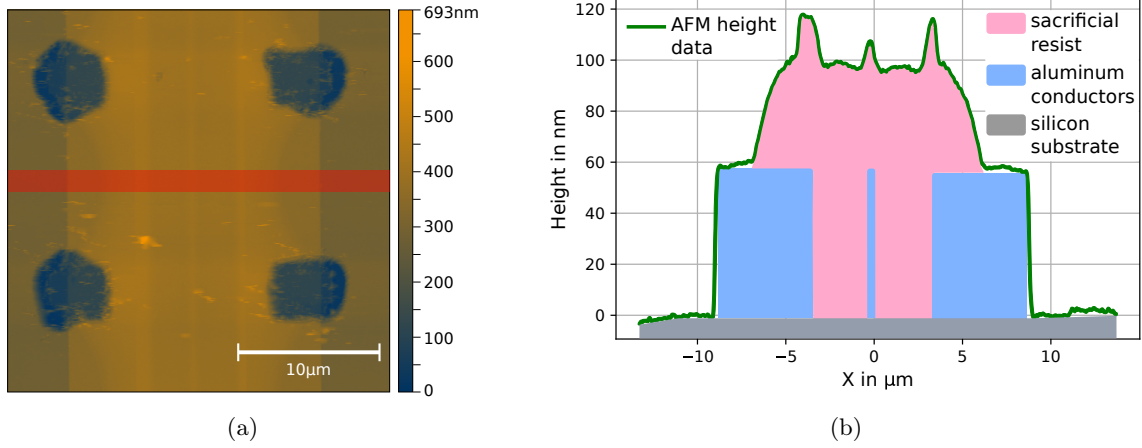
at the surface of the ground plane can be attributed to the underlying layers, namely the metal conductors and the sacrificial resist.

If one follows the height data from outside towards the center of the tunnel in fig. 6.5b, the first increase can be attributed to the two metal strips on both sides of the central conductor. The following smooth increase in height comes from the rounded profile of the sacrificial resist thanks to the proximity effect (see section 4.2.2). After the smooth increase, the height profile rises sharply again, indicating where the resist was directly exposed. A rapid drop in the height profile shows the inner edge of the two metal strips. The resist thickness, however, takes its maximum value of almost 100 nm here. This difference of approximately 20 nm with respect to the resist thickness on unpatterned surfaces shows the influence, that the local structures have on resist deposited by spin coating. The aluminum central conductor in the center of the tunnel leads to a renewed increase in height. This rise, however, is smaller than the thickness of the aluminum layer, leading to an effective thickness of the resist on top of the central conductor of approximately 50 nm to 60 nm. This height is particularly relevant for the microwave properties of the transmission lines, as it affects the capacitance.

The imaging analysis presented in this section enabled the visualization of the sample and also quantitative measurements of the dimensions of the fabricated structures. Especially useful was the AFM measurement, as it also provided information about the inner profile of the vacuum-gap microstrip tunnels. Also, defects and imperfections could be identified using the described imaging methods. To assess the microwave performance of the fabricated transmission lines, however, measurements at cryogenic temperatures are necessary.
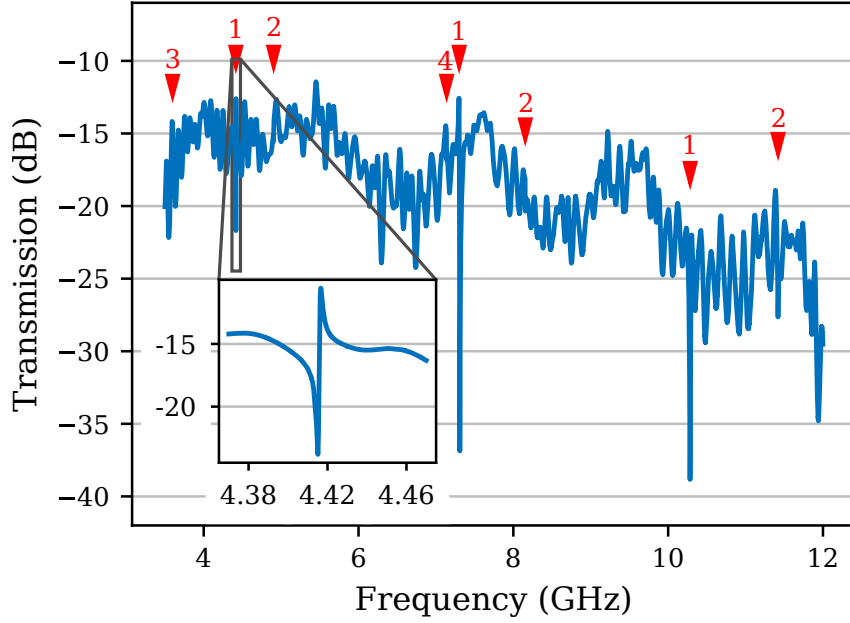
Figure 6.6: Uncalibrated VNA transmission spectrum of the feed line coupled to the vacuum-gap microstrip resonators. The observed resonances are harmonics of the fundamental frequencies. The inset shows a zoom on one of the resonances. The locations of all resonances that have been analyzed are indicated by the red markers; the number above corresponds to the set they belong to (see table 6.1).

6.2 Cryogenic Measurements

After finishing the fabrication process and mounting in a sample holder, the fabricated chips were measured at cryogenic temperatures in a dilution refrigerator. The data discussed in the following is obtained by VNA transmission measurements. For the detailed measurement setup see section 5.4.

6.2.1 Resonant Frequencies

To identify the individual resonances in the transmission spectrum of the feed lines, first, a broadband spectrum was taken. The spectrum for the vacuum-gap microstrip resonators (fig. 6.6) and the bridged CPW resonators (fig. 6.7) are obtained from different sample chips in different cool-downs. This was necessary because the feed line, coupled to the bridged CPW resonators, did not show transmission (i.e. was broken or shorted) for the first cool-down and the same is true for the feed line with the vacuum-gap microstrip resonators in the second cool-down.

Nevertheless, meaningful data could be obtained, capable of quantifying the performance and thereby demonstrating the potential of the newly developed vacuum-gap microstrip transmission lines and the air-bridges.

Table 6.1: Resonance frequencies in GHz observed in the transmission of the feed line coupled to the vacuum-gap microstrip resonators. The resonances have been grouped into sets according to the fundamental frequency they stem from. The fundamental frequencies were not observed directly but extracted from the observed ones via eq (6.2.1).

Set \ Mode	$i = 1$	$i = 2$	$i = 3$	fundamental $i = 0$
set 1	4.42	7.30	10.28	1.47
set 2	4.90	8.15	11.42	1.63
single 3	3.60[1]			1.20[1]
single 4		7.14[1]		1.43[1]

Vacuum-Gap Microstrip Resonators

The transmission spectrum of the feed line coupled to the vacuum-gap microstrip resonators is shown in fig. 6.6. The observed resonant dips in the spectrum are listed in table 6.1. However, the appearing resonances outnumber the resonators and their spacing and positions do not match the design values. What we observe are higher modes, indicating that the fundamental frequencies of the fabricated resonators are significantly below the design values and thereby also outside our measurement range (3.5 GHz to 12 GHz). We can conclude this from comparing the resonances and grouping them according to their fundamental frequency.

In section 3.1.2 we introduced the quarter-wave resonator and noted, that in contrast to a lumped-element realization, such distributed resonators support higher modes. Due to the boundary conditions of a quarter-wave resonator, the frequencies of the higher modes are given by

$$f_i = (2i + 1) \cdot f_{\mathrm{r}}. \tag{6.2.1}$$

Here $f_0 = f_{\mathrm{r}}$ is the fundamental frequency and f_i is the frequency of the i-th higher mode. From this equation we obtain the relative factors between the frequencies of higher modes. So we expect for example the second higher mode to differ from the first one by a factor of $\frac{5}{3}$, and the first from the fundamental by a factor of 3. This is the key in identifying the observed resonances as higher modes of a fundamental frequency. For example, one can see that resonance No 5 differs from resonance No 2 by a factor of approximately $\frac{5}{3}$. From resonance No 5 to resonance No 7 it is a factor of $\frac{7}{5}$. We find that the majority of the observed resonances belong to two sets originating from two fundamental frequencies at 1.47 GHz and 1.63 GHz as shown in table 6.1.

For the two remaining resonances at 3.6 GHz and 7.14 GHz we are not able to observe the set of higher modes they are part of. That we do not see those other modes is likely due to under-coupling. As the coupling observed for these two resonances is low ($Q_{\mathrm{c}} \approx 5 \times 10^4$ to 3×10^5), the resonances are hard to observe as they are vanishing in the strong background variation. The impact of the coupling even gets worse, as the internal quality factors Q_{int} decrease with increasing frequency leading to even bigger under-coupling. Finally, the coupling does depend on the frequency as standing wave patterns and the resulting electric field distribution along the feed line affects the

---

[1] Mode number assignment and resulting fundamental frequency based on comparison with sets 1 and 2

Table 6.2: Designed and observed resonant frequencies and coupling strengths of the bridged CPW resonators. The errors given with the coupling quality factors Q_c are estimated from the variation of the fitting results.

Resonator No	1	2	3	4	5
observed f_r in GHz	4.86	5.30	5.68	6.06	6.57
designed f_r in GHz	6	6.5	7	7.5	8
coupler type	parallel-plate	parallel-plate	parallel-plate	coplanar	coplanar
observed Q_c	$2.1(2) \times 10^4$	$2.7(2) \times 10^4$	$2.8(2) \times 10^4$	$2.1(3) \times 10^5$	$8(1) \times 10^5$
designed Q_c	10^3	10^4	10^5	10^5	10^6

coupling strengths of the resonators. These effects combined can easily lead to the resonant dips vanishing.

Assuming that the two extra frequencies are indeed part of a set of higher modes, we can again extract the fundamental frequency. The second assumption we use is, that the fundamental frequency will be similar to the ones already extracted from set 1 and set 2. With this we can identify the most plausible order i of the resonances and calculate back to the fundamental frequencies from there. We obtain 1.2 GHz and 1.43 GHz, which together with the basic frequencies from set 1 and set 2 resemble four of the five designed frequencies, consistently shifted to approximately $\frac{1}{5}$ of their design value.

The reason why we observe such a large shift towards smaller frequencies is because of kinetic inductance. While during designing the resonators kinetic inductance was not taken into account, later considerations and simulations showed that it can not be neglected. To which degree kinetic inductance influences the fabricated resonators becomes apparent, when the temperature dependence of the resonators is examined in section 6.2.3. In addition to the kinetic inductance, part of the shift in frequencies is also due to the increased capacitance because of the smaller height of the tunnels (see section 6.1.2).

The fifth resonator, for which no resonances are observed is likely completely under-coupled. The design predicts a coupling quality factor of $Q_c = 10^6$ for the weakest coupled resonator which is much higher than the quality factors observed and discussed in the next section.

All things considered, we were able to observe four of the designed five resonators on the chip. Although the resonances are shifted below the measurement range by kinetic inductance, we could still identify them by their higher modes. The absence of some of these higher modes and the entire set of resonances stemming from the fifth resonator can likely be attributed to under-coupling of the resonators and to the strong background variation, making the resonances hard to observe.

Bridged CPW Resonators

The spectrum of the feed line connected to the five resonators in bridged CPW design is shown in fig. 6.7. In contrast to the data from the vacuum-gap microstrips, the feed line shows a higher level of transmission. The difference of approximately 10 dB comes from either the on-chip feed line itself,
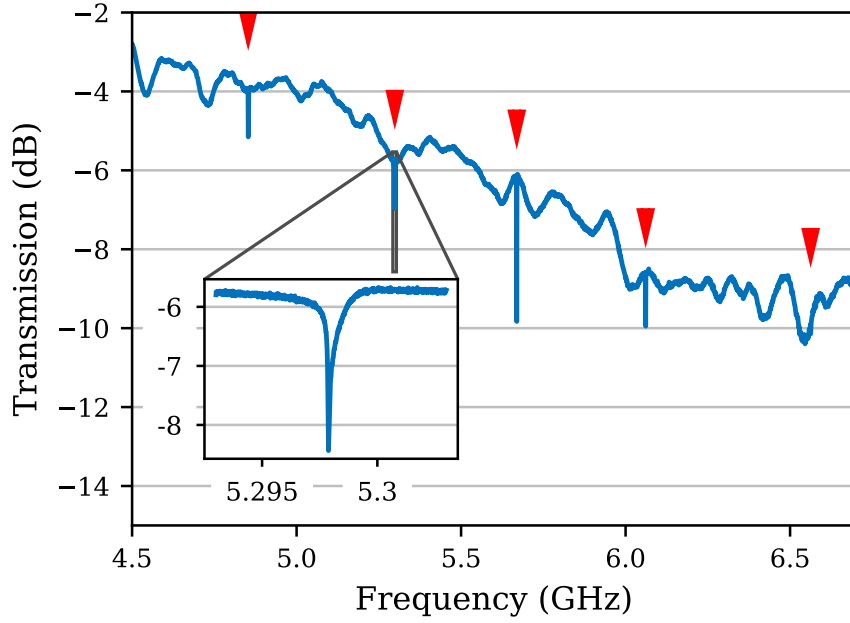
Figure 6.7: Uncalibrated VNA transmission spectrum of the feed line coupled to the bridged CPW resonators. The inset shows a zoom on one of the resonances. The locations of all resonances that have been analyzed are indicated by the red markers.

which might show increased loss due to fabrication defects, or to a faulty connection between the switch and the sample chip.

Also in contrast to the vacuum-gap microstrip resonators, all resonators realized in the bridged CPW design can be observed. The resonance frequencies of the resonators are again obtained by circle-fitting and presented in table 6.2. While they are collectively appearing at approximately $\frac{4}{5}$ of their designed frequency, the spacings between them remain unaltered and only scaled down accordingly. From these observations we can conclude, that the air-bridges are not collapsed along the length of the resonators, as this would lead to a short and thereby to a significantly shifted resonant frequency. Small shifts of the resonators with respect to each other can be explained with the different coupling strengths, which shift the resonant frequencies (see section 3.1.2) and by parasitic capacitance between the couplers and the ground plane.

The collective shift to lower frequencies, which is observed for all resonators, can also partly be attributed to coupling and parasitic capacitance of the coupling structures. Another factor that plays a role here is again the height of the tunnel structures, which turns out to be less than the estimated value used for the design of the resonators (see section 6.1.2). Here it is important to remember, that, although the bridges only cover about 9 % of the length of the CPW resonators, they still account for a significant part of their overall capacitance.
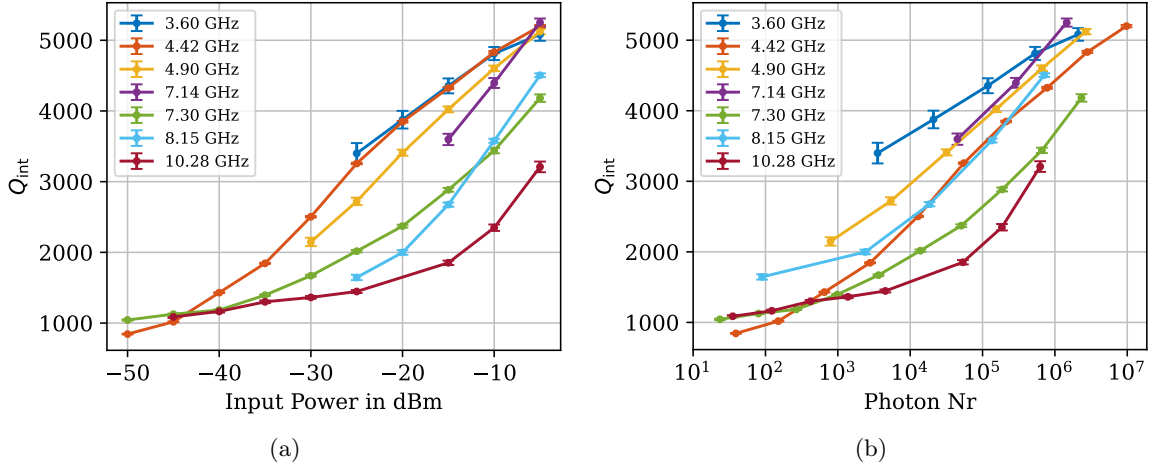
Figure 6.8: Internal quality factors of the vacuum-gap microstrip resonators as obtained by circle fitting of the transmission data of the feed line. The lines between the points are a guide for the eye. All resonances were analyzed for all input powers in the interval $-50\,\mathrm{dBm}$ to $-10\,\mathrm{dBm}$ in steps of $5\,\mathrm{dBm}$. Where points are missing with regard to this scheme, no reliable fits could be obtained. The data is plotted over applied input power in **(a)** and over the number of photons in the resonator in **(b)**. The error bars represent the statistical uncertainties of the fits.

6.2.2 Q-Factor

To quantify the performance of the fabricated transmission lines we examine the internal quality factor Q_{int} that is connected to the loss tangent $\tan\delta$ via $Q_{\mathrm{int}} = \frac{1}{\tan\delta}$ (see section 3.1.3). This property is essential for the use in traveling wave parametric amplifiers, as the dielectric losses often limit their noise performance [17].

The microwave properties of the resonators are extracted from the transmission data via circle fitting (see sec. 3.1.4). The circle fit routine returns the resonance frequencies as well as the internal (Q_{int}) and coupling (Q_{c}) quality factors. The statistical uncertainty of these values is used for the error bars of the data presented in figures 6.8 and 6.9. The circle fitting was done for all observed resonances and for different input powers. However, meaningful fits could not be obtained for all resonances at all input powers. This is especially true for the under-coupled resonators which become less prominent when the power is reduced. Those data points are not shown in the plots and are excluded from further analysis. For the vacuum-gap microstrip resonance at $11.42\,\mathrm{GHz}$ reliable fits could not be obtained for any of the input powers, because of the already mentioned strong under-coupling and background variation.

Vacuum-Gap Microstrip Resonators

The quality factors for the resonators in vacuum-gap microstrip geometry are shown in fig. 6.8a. We observe quality factors from 1000 for low powers up to 3000 to 5000 for the highest powers tested. This increase is expected as a result of the saturation of two-level-systems (TLS) at the surfaces and interfaces of the resonators [81]. The quality factors are likely limited by sacrificial resist, that is still left inside the tunnels, or by defects on the inner side of the tunnel.

Also, we can observe that the quality factors for higher frequencies tend to be lower than for lower frequencies. This is likely linked to increased dielectric loss for higher frequencies. Also it could be related to the higher frequencies corresponding to higher modes of the quarter-wave resonators.

In fig. 6.8b the same data with the x-axis converted from power to the average number of photons in the resonators (see section 3.1.5) is presented. This assumes the aforementioned fridge attenuation of 60 dB. However, it is important to note that this attenuation is what is typically measured in our fridge, but can change with the specific setup and also with frequency. Unfortunately, the calibration of the attenuation is complicated in a dilution refrigerator like ours and was not done for this cool-down. Any additional attenuation occurring before the resonators will decrease the actual number of photons present in the resonators. So the numbers given on the x-axis of fig. 6.8b can be taken as an upper bound for the number of photons in the resonators.

It is in fact very likely that we are facing extra attenuation before the vacuum-gap microstrip resonators, not only because of the difference observed in the transmission but also because of the measured quality factors. The two panels from fig. 6.8 shows increasing quality factors for increasing power, but also a flattening of this trend for the lowest observed powers. This indicates that we are in fact in the low-power regime, although from the calculations we could still have as many as 100 photons in the resonators.

With the observed internal quality factors for the vacuum-gap microstrip resonators, we have shown, that this new fabrication technique can compete with established state-of-the-art microstrip designs which use a dielectric. The obtained low-power internal quality factor $Q_{\text{int}} \approx 1000$ translates into a loss tangent of $\tan\delta = \frac{1}{Q_{\text{int}}} \approx 1 \times 10^{-3}$. With that value, it places itself within the range of quality factors of transmission lines that have already been successfully deployed in TWPAs (see table 2.1 in chapter 2). With the shown performance and the perspective of further improvement of this technique, the fabrication method is suitable for deployment in a TWPA and worth further development and investigation.

Bridged CPW Resonators

For the bridged CPW resonators, we obtain higher quality factors, ranging from 20 000 in the low power regime up to 30 000 to 60 000 for higher powers, as shown in fig. 6.9. This agrees with what was stated before, namely that the vacuum-gap microstrip transmission line resonators are limited by the tunnel structure and any sacrificial resist residue left behind by the plasma etching.

Like for the vacuum-gap microstrip resonators, we also see decreasing quality factors for increasing frequencies for the bridged CPW resonators. As before this might be because of the frequency dependence of the dielectric loss limiting the performance of the resonators. Also, the coupling of the resonators can play a role here. Part of the reduced internal quality factor for the resonators No 4 and especially No 5 might be because of the under-coupling, leading to less reliable results of the circle fits.
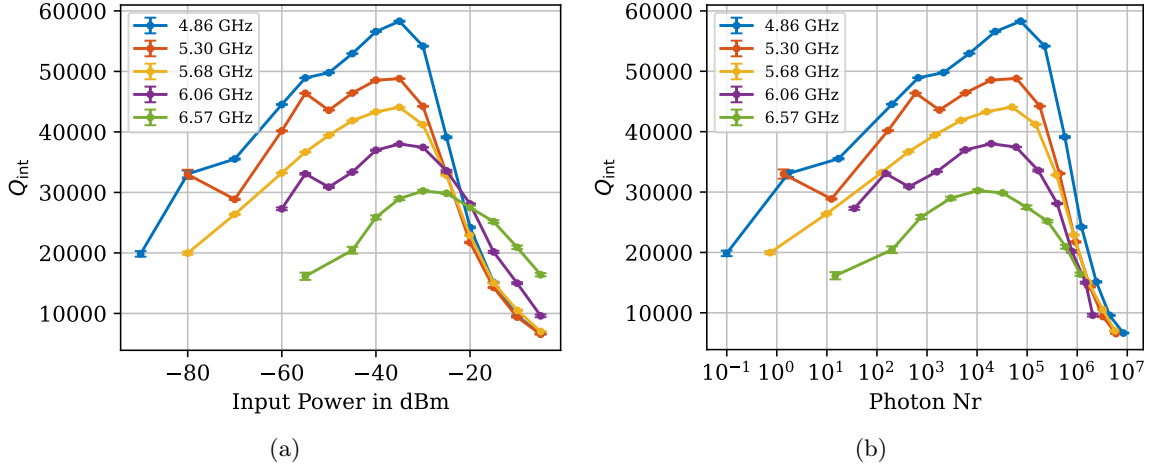
Figure 6.9: Internal quality factors of the bridged CPW as obtained by circle fitting the transmission spectrum of the feed line. The lines between the points are a guide for the eye. All resonances were analyzed for all input powers in the interval $-90\,\mathrm{dBm}$ to $-5\,\mathrm{dBm}$ in steps of $5\,\mathrm{dBm}$. Where points are missing with regard to this scheme, no reliable fits could be obtained. The data is plotted over applied input power in **(a)** and over the number of photons in the resonator in **(b)**. The error bars represent the statistical uncertainties of the fits.

At input powers of $-35\,\mathrm{dBm}$ to $-30\,\mathrm{dBm}$ the quality factor starts to drop rapidly with increasing power. Especially when looking at the photon-number representation in fig. 6.9b, this drop in quality factor seems to occur at the same number of photons ($\approx 10^5$) for all resonators. This effect is not yet well understood and will require further investigation.

It is important to stress once more, that the data for the vacuum-gap microstrip and the bridged CPW resonators were taken in different cool-downs. The transmission data shown in fig. 6.6 and fig. 6.7 implies the presence of additional losses in the signal path of the vacuum-gap microstrip resonators. Again, the numbers given for the photon number in the resonators can be seen as an upper bound. The fact, that lower powers could be examined for the bridged CPW resonators is likely due to the extra non-accounted-for loss in the vacuum-gap microstrip resonators, as well as due to the fact that the CPW resonators show higher quality factors and therefore more pronounced resonant dips.

Because of the higher quality factors of the bridged CPW resonators, the better fits of the resonances, and the unambiguous identification of the resonators, we can have a closer look at the achieved coupling. As already mentioned in section 5.4.1, the chip that was examined showed defects at the parallel-plate couplers. Those were lifted up, above their design height, which should result in weaker coupling. Like the internal quality factors, also the coupling quality factors were obtained by circle fitting. In table 6.2 they are presented next to their design values. When the internal quality factor of the resonators changes with applied power, also the coupling quality factors yielded by the circle fit change. This is probably due to the changing ratio between Q_{int} and Q_{c}, as the fitting routine works best when the two quality factors are comparable and yields less reliable results for strong under- or over-coupling. This variation of coupling quality factors for different powers was used to estimate the uncertainties of the presented values. One can observe, that all three parallel-
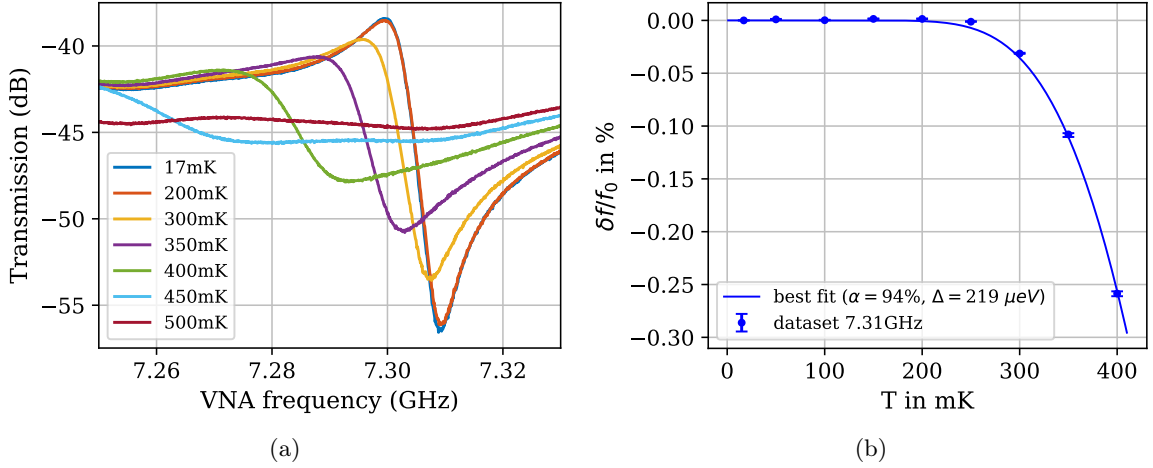
Figure 6.10: The resonant frequency of a resonator with kinetic inductance shifts to lower frequency with increasing temperature. **(a)** Resonant dip in the feed line transmission spectrum for a vacuum-gap microstrip resonator at different temperatures. **(b)** Relative shift in resonance frequency over temperature. The data is fitted with equation (6.2.2) to extract the kinetic inductance ratio α. The error bars represent the statistical uncertainties of the fits.

plate couplers show similar coupling quality factors. This is likely due to the fact, that with the parallel-plate part of the coupler much further away from the feed line than designed, the coupling is dominated by the capacitance between the larger coplanar parts of the couplers. The influence of this extra capacitance is also responsible for the smaller-than-designed coupling quality factor of resonator No 3.

Because of their entirely coplanar design, the couplers of resonators No 4 and No 5 are closer to their respective design values. However, as the coupling is very weak for them, the numerical value has to be interpreted cautiously. Again, the argument is, that circle fitting yields the most reliable results when Q_{int} and Q_{c} are comparable.

6.2.3 Temperature-Dependence and Kinetic Inductance

For the vacuum-gap microstrip resonators, also the dependence on temperature was investigated. A change of the quality factor and of resonant frequency is expected as the temperature of the aluminum increases and gets closer to its critical temperature leading to an increase in quasi-particles in it. The frequency shift can be used to estimate the contribution of kinetic inductance to the total inductance of the resonator (see sec. 3.2.2).

The temperature was swept up to 550 mK in steps of 50 mK. After a thermalization time of 30 min after each warming up step, all eight observed resonances listed in table 6.1 were measured, using moderate probing power of −20 dBm at the input of the fridge.

The resulting transmission data is shown in fig. 6.10a. As before, the figure includes error bars given by the circle fit errors. Starting from approximately 300 mK, the resonance feature is getting shallower and shifts towards lower frequencies with increasing temperature.

For the quantitative analysis of the temperature dependence, only the resonance at 7.3 GHz was used, as for this one reliable results up to a temperature of 400 mK could be obtained. Because of the strong coupling for this resonator and at this frequency in particular, the resonant dip in the transmission spectrum remains visible when the internal quality factor decreases with increasing temperature. For the other resonances, reliable fits were only possible for the lower temperatures, where the change in resonance frequency is small compared to the change at higher temperatures. In fig. 6.10b the decrease in resonance frequency is plotted over temperature. The data is fitted with an approximation to the Mattis-Bardeen theory, as explained in section 3.2.2. The function used relates the relative shift in frequency to the temperature T and the superconducting energy gap Δ

$$\frac{\delta f_{\mathrm{r}}}{f_{\mathrm{r}}(T=0)} = -\frac{\alpha}{2}\sqrt{\frac{\pi\Delta}{2k_{\mathrm{B}}T}}\exp\left(-\frac{\Delta}{k_{\mathrm{B}}T}\right). \tag{6.2.2}$$

The values obtained by the fit are the kinetic inductance ratio $\alpha = 0.94(15)$ and a superconducting gap of $\Delta = 219(6)\,\mu\mathrm{eV}$. The given errors represent the statistical uncertainties of the fit. It is worth noting, that of course $\alpha > 1$ would be unphysical and its fitting range was restricted to the interval between 0 and 1. The result for Δ is consistent with what is usually observed for thin aluminum films [82]. However, it has still to be interpreted cautiously, as the fit parameters are strongly dependent on the last points of fig. 6.10b and thereby on the circle fits of the transmission data at the highest temperatures, where the resonance dip is the least pronounced. These uncertainties are not accounted for by the statistical errors given as error bars in the figure. This becomes obvious when comparing the fit from fig. 6.10b to the data. Some of the data points differ from the fit by significantly more than their statistical error bars.

In any case, however, the fit confirms the hypothesis, that the resonance frequencies of the vacuum-gap microstrip resonators are shifted down because of the large amount of kinetic inductance present in the central conductors. With the kinetic inductance fraction obtained from the fit, we would expect the resonance frequencies of the resonators to be well below the designed values. In fact, we expect a reduction by a factor of $\sqrt{1-\alpha} \approx \frac{1}{4}$ with respect to the design value, for which only the geometric inductance was taken into account. This factor is obtained by considering the total inductance L as the sum of geometric inductance L_{geom} and kinetic inductance L_{kin}

$$L = L_{\mathrm{geom}} + L_{\mathrm{kin}} \tag{6.2.3}$$

$$\Leftrightarrow L = L_{\mathrm{geom}} + \alpha L \tag{6.2.4}$$

$$\Leftrightarrow L = \frac{L_{\mathrm{geom}}}{1-\alpha}, \tag{6.2.5}$$

and inserting this result into dependence of the resonant frequency of an LC-resonator on the inductance L (see section 3.1.2)

$$f_{\mathrm{r}} \propto \frac{1}{\sqrt{L}} = \frac{\sqrt{1-\alpha}}{\sqrt{L_{\mathrm{geom}}}}. \tag{6.2.6}$$

Coming back to the basic frequencies extrapolated from the higher modes of the resonators as listed

in table 6.1, this factor can explain the observed shifts.

To further confirm our results, the data was also fitted with a slightly different routine, as used and described in [83], yielding a kinetic inductance ratio of $\alpha = 0.73(11)$ and a superconducting gap of $\Delta = 209(5)\,\mu\text{eV}$ with a qualitatively very similar fit. Again, the errors given are merely the statistical fit errors, The conclusion we draw from the two results is that the kinetic inductance of the narrow central conductors is important for the resonance frequency of our resonators. To confidently give a specific value of α with reliable error bounds, however, the analyzed data is not sufficient.

The cryogenic measurement has enabled quantitative analysis of the performance of the structures fabricated in the vacuum-gap microstrip design. Although the fundamental resonances were outside the measurement range because of the kinetic inductance of the central conductors, still four out of five resonators could be identified thanks to their higher modes. With low-power quality factors of around 1000, they can compete with thin-film dielectric microstrip transmission lines, as they are already deployed in TWPAS. For the bridged CPW resonators fabricated with the same fabrication process, we obtain higher low-power quality factors of approximately 20 000. The temperature dependence of the vacuum-gap microstrip resonators was used to extract the kinetic inductance ratio and thereby confirm that the kinetic inductance is indeed the reason for the shift in frequency.

Chapter 7

Conclusion and Outlook

The goal of this thesis was to develop a fabrication process for high-capacitance, low-loss transmission lines. This we have achieved in an elaborate multi-layer fabrication process for a vacuum-gap tunnel-like microstrip structure, which we call the vacuum-gap microstrip. This structure is built up by a base layer, a layer of sacrificial resist as a placeholder, and a ground plane on top. Holes are patterned and etched into the ground plane to access the sacrificial resist filling the tunnels. Through those access points, the resist is removed with an isotropic O_2 plasma etch, leaving the desired free-standing vacuum-gap microstrip structure.

During the development of the fabrication process, a series of challenges had to be overcome. Notably, the evaporation of the ground plane introduced excessive strain, so a sputtering process had to be adapted for the specific tools available to us. Also, the creation of the hard mask for the plasma etching, as well as the plasma etching of the holes itself proved to be particularly complicated, due to the non-planar relief of the tunnels and their fragility. Moreover, smaller issues like the alignment between layers, non-sufficient adhesion of the sacrificial resist, or accurate and reliable dicing of the sample chips needed to be addressed. In the end, the fabrication process could be realized with standard methods compatible with many materials commonly used in the superconducting circuits community. It is also worth noting, that no high-temperature steps are necessary for the construction of the vacuum-gap microstrips.

For testing the performance of the vacuum-gap microstrips and the air-bridges that can be realized with the same process, quarter-wave resonators were fabricated and measured in a dilution refrigerator. The low-power quality factors of $Q_{\text{int}} = 1000$ or the dielectric loss tangent of $\delta = 10^{-3}$ respectively, place our structures well within the performance range that state of the art microstrip transmission lines, as they are already used for microwave TWPAs, are able to achieve. The limiting factor of the performance of the vacuum-gap microstrip resonators is likely resist residue or defects in the tunnel.

With further improvement of the line design and the fabrication process, we expect to be able to enhance the performance of the vacuum-gap microstrips. Especially modifications of the hole design and the mask creation process needed for hole etching promise to achieve more thorough resist removal and overall cleaner edges and surfaces. Closer investigation of the ground plane deposition step and potential defects on the inner wall of the tunnels will also be worth the effort.

The intended use case for such high capacitance transmission lines with comparably low loss is the deployment in traveling wave parametric amplifiers. There, high capacitance is needed to counteract the high kinetic inductance necessary for efficient amplification. Low losses are essential to allow for amplification near the quantum limit of added noise.

To realize the goal of a TWPA, however, still a number of different issues will have to be addressed. For one thing, these will be the implementation of the mentioned improvements of the fabrication process and the testing of its reproducibility. Further, we will continue by realizing the central conductors of the resonators in granular aluminum. The optimization of a deposition process for this high kinetic inductance material in our facility will be the next step towards building a quantum-limited TWPA.

Apart from the use in a TWPA, the developed fabrication process or variations of it could also be used in a number of different applications. The use as air-brides over coplanar structures has already been demonstrated in this thesis. These bridges can be used to ensure good ground plane connection or to realize strong capacitive couplings. In addition to that, they could be used to realize on-chip lumped-element capacitors with a small footprint, or, together with a highly inductive central conductor, to create slow-light transmission lines.

Bibliography

[1] R. P. Feynman. "Simulating physics with computers". In: *International Journal of Theoretical Physics* 21.6 (June 1982).

[2] S. S. Gill et al. "Quantum computing: A taxonomy, systematic review and future directions". In: *Software: Practice and Experience* 52.1 (2022).

[3] F. Arute et al. "Quantum supremacy using a programmable superconducting processor". In: *Nature* 574.7779 (Oct. 2019).

[4] J. M. Pino et al. "Demonstration of the trapped-ion quantum CCD computer architecture". In: *Nature* 592.7853 (Apr. 2021).

[5] S. Krinner et al. "Realizing Repeated Quantum Error Correction in a Distance-Three Surface Code". In: *arXiv:2112.03708 [cond-mat, physics:quant-ph]* (Dec. 2021).

[6] M. Cerezo et al. "Variational Quantum Algorithms". In: *Nature Reviews Physics* (2021).

[7] F. Jazaeri et al. "A Review on Quantum Computing: From Qubits to Front-end Electronics and Cryogenic MOSFET Physics". In: *2019 MIXDES - 26th International Conference "Mixed Design of Integrated Circuits and Systems"*. June 2019.

[8] H.-L. Huang et al. "Superconducting quantum computing: a review". In: *Science China Information Sciences* 63.8 (July 2020).

[9] C. M. Caves. "Quantum limits on noise in linear amplifiers". In: *Physical Review D* 26.8 (Oct. 1982).

[10] J. Aumentado. "Superconducting Parametric Amplifiers: The State of the Art in Josephson Parametric Amplifiers". In: *IEEE Microwave Magazine* 21.8 (Aug. 2020).

[11] M. A. Castellanos-Beltran. "Development of a Josephson Parametric Amplifier for the Preparation and Detection of Nonclassical States of Microwave Fields". PhD thesis. 2002.

[12] M. A. Castellanos-Beltran and K. W. Lehnert. "Widely tunable parametric amplifier based on a superconducting quantum interference device array resonator". In: *Applied Physics Letters* 91.8 (Aug. 2007).

[13] M. A. Castellanos-Beltran et al. "Amplification and squeezing of quantum noise with a tunable Josephson metamaterial". In: *Nature Physics* 4.12 (Dec. 2008).

[14] N. Bergeal et al. "Phase-preserving amplification near the quantum limit with a Josephson ring modulator". In: *Nature* 465.7294 (May 2010).

[15] I. Siddiqi et al. "RF-Driven Josephson Bifurcation Amplifier for Quantum Measurement". In: *Physical Review Letters* 93.20 (Nov. 2004).

[16] A. A. Clerk et al. "Introduction to quantum noise, measurement, and amplification". In: *Reviews of Modern Physics* 82.2 (Apr. 2010).

[17] M. Esposito et al. "Perspective on traveling wave microwave parametric amplifiers". In: *Applied Physics Letters* 119.12 (Sept. 2021).

[18] N. Zobrist et al. "Wide-band parametric amplifier readout and resolution of optical microwave kinetic inductance detectors". In: *Applied Physics Letters* 115.4 (July 2019).

[19] B. Ho Eom et al. "A wideband, low-noise superconducting amplifier with high dynamic range". In: *Nature Physics* 8.8 (Aug. 2012).

[20] C. Bockstiegel et al. "Development of a Broadband NbTiN Traveling Wave Parametric Amplifier for MKID Readout". In: *Journal of Low Temperature Physics* 176.3 (Aug. 2014).

[21] M. R. Vissers et al. "Low-noise kinetic inductance traveling-wave amplifier using three-wave mixing". In: *Applied Physics Letters* 108.1 (Jan. 2016).

[22] L. Ranzani et al. "Kinetic inductance traveling-wave amplifiers for multiplexed qubit readout". In: *Applied Physics Letters* 113.24 (Dec. 2018).

[23] C. Macklin et al. "A near–quantum-limited Josephson traveling-wave parametric amplifier". In: *Science* 350.6258 (Oct. 2015).

[24] T. C. White et al. "Traveling wave parametric amplifier with Josephson junctions using minimal resonator phase matching". In: *Applied Physics Letters* 106.24 (June 2015).

[25] A. B. Zorin et al. "Traveling-Wave Parametric Amplifier Based on Three-Wave Mixing in a Josephson Metamaterial". In: *2017 16th International Superconductive Electronics Conference (ISEC)*. June 2017.

[26] A. Miano and O. A. Mukhanov. "Symmetric Traveling Wave Parametric Amplifier". In: *IEEE Transactions on Applied Superconductivity* 29.5 (Aug. 2019).

[27] W. Shan, Y. Sekimoto, and T. Noguchi. "Parametric Amplification in a Superconducting Microstrip Transmission Line". In: *IEEE Transactions on Applied Superconductivity* 26.6 (Sept. 2016).

[28] L. Planat et al. "Photonic-Crystal Josephson Traveling-Wave Parametric Amplifier". In: *Physical Review X* 10.2 (Apr. 2020).

[29] A. Ranadive et al. "A reversed Kerr traveling wave parametric amplifier". In: *arXiv:2101.05815 [cond-mat, physics:quant-ph]* (Jan. 2021).

[30] S. Goldstein et al. "Four wave-mixing in a microstrip kinetic inductance travelling wave parametric amplifier". In: *Applied Physics Letters* 116.15 (Apr. 2020).

[31] S. Shu et al. "Nonlinearity and wideband parametric amplification in an NbTiN microstrip transmission line". In: *Physical Review Research* 3.2 (June 2021).

[32] M. Malnou et al. "Three-Wave Mixing Kinetic Inductance Traveling-Wave Amplifier with Near-Quantum-Limited Noise Performance". In: *PRX Quantum* 2.1 (Jan. 2021).

[33] S. Chaudhuri et al. "Broadband parametric amplifiers based on nonlinear kinetic inductance artificial transmission lines". In: *Applied Physics Letters* 110.15 (Apr. 2017).

[34] A. A. Adamyan et al. "Superconducting microwave parametric amplifier based on a quasi-fractal slow propagation line". In: *Journal of Applied Physics* 119.8 (Feb. 2016).

[35] J. Hansryd et al. "Fiber-based optical parametric amplifiers and their applications". In: *IEEE Journal of Selected Topics in Quantum Electronics* 8.3 (May 2002).

[36] M. E. Marhic. *Fiber Optical Parametric Amplifiers, Oscillators and Related Devices*. Cambridge: Cambridge University Press, 2007.

[37] B. D. Josephson. "Possible new effects in superconductive tunnelling". In: *Physics Letters* 1.7 (July 1962).

[38] M. Tinkham. *Introduction to Superconductivity*. Dover Books on Physics Series. Dover Publications, 2004.

[39] H. Rotzinger et al. "Aluminium-oxide wires for superconducting high kinetic inductance circuits". In: *Superconductor Science and Technology* 30.2 (Nov. 2016).

[40] L. Planat et al. "Fabrication and Characterization of Aluminum SQUID Transmission Lines". In: *Physical Review Applied* 12.6 (Dec. 2019).

[41] E. Dumur. "A V-shape superconducting artificial atom for circuit quantum electrodynamics". PhD thesis. Université Grenoble Alpes, Feb. 2015.

[42] N. H. L. Koster et al. "Investigations on Air Bridges Used for MMICs in CPW Technique". In: *1989 19th European Microwave Conference*. Sept. 1989.

[43] J. Lee et al. "Suppression of coupled-slotline mode on CPW using air-bridges measured by picosecond photoconductive sampling". In: *IEEE Microwave and Guided Wave Letters* 9.7 (July 1999).

[44] F. Boussaha et al. "Development of TiN Vacuum-Gap Capacitor Lumped-Element Kinetic Inductance Detectors". In: *Journal of Low Temperature Physics* 199.3 (May 2020).

[45] K. Cicak et al. "Low-loss superconducting resonant circuits using vacuum-gap-based microwave components". In: *Applied Physics Letters* 96.9 (Mar. 2010).

[46] W. Shan, Y. Sekimoto, and T. Noguchi. "Microwave loss of DC sputtered NbTiN microstrip lines". In: *Japanese Journal of Applied Physics* 54.9 (Aug. 2015).

[47] J. Gao et al. "Experimental evidence for a surface distribution of two-level systems in superconducting lithographed microwave resonators". In: *Applied Physics Letters* 92.15 (Apr. 2008).

[48] C. R. H. McRae et al. "Materials loss measurements using superconducting microwave resonators". In: *Review of Scientific Instruments* 91.9 (Sept. 2020).

[49] C. Deng, M. Otto, and A. Lupascu. "Characterization of low-temperature microwave loss of thin aluminum oxide formed by plasma oxidation". In: *Applied Physics Letters* 104.4 (Jan. 2014).

[50] G. Calusine et al. "Analysis and mitigation of interface losses in trenched superconducting coplanar waveguide resonators". In: *Applied Physics Letters* 112.6 (Feb. 2018).

[51] D. Pozar. *Microwave Engineering, 4th Edition.* Wiley, 2011.

[52] A. Megrant et al. "Planar superconducting resonators with internal quality factors above one million". In: *Applied Physics Letters* 100.11 (Mar. 2012).

[53] J. Gao. "The Physics of Superconducting Microwave Resonators". PhD thesis. California Institute of Technology, 2008.

[54] D. Zoepfl et al. "Characterization of low loss microstrip resonators as a building block for circuit QED in a 3D waveguide". In: *AIP Advances* 7.8 (Aug. 2017).

[55] A. Bruno et al. "Reducing intrinsic loss in superconducting resonators by surface treatment and deep etching of silicon substrates". In: *Applied Physics Letters* 106.18 (May 2015).

[56] R. Barends. "Photon-detecting superconducting resonators". PhD thesis. Delft University of Technology, 2009.

[57] A. J. Annunziata et al. "Tunable superconducting nanoinductors". In: *Nanotechnology* 21.44 (Oct. 2010).

[58] R. Meservey and P. M. Tedrow. "Measurements of the Kinetic Inductance of Superconducting Linear Structures". In: *Journal of Applied Physics* 40.5 (Apr. 1969).

[59] J. P. Turneaure, J. Halbritter, and H. A. Schwettman. "The surface impedance of superconductors and normal conductors: The Mattis-Bardeen theory". In: *Journal of Superconductivity* 4.5 (Oct. 1991).

[60] T. Tai, J. Cai, and S. M. Anlage. "Coherence Time Enhancement of Interacting Two-Level Systems in Aluminum Superconducting Resonators". In: *arXiv:2109.11742 [cond-mat, physics:quant-ph]* (Sept. 2021).

[61] M. Féchant. "Non-linear lattices of granular aluminium resonators". PhD thesis. Université Paris-Saclay, May 2021.

[62] R. W. Cohen and B. Abeles. "Superconductivity in Granular Aluminum Films". In: *Physical Review* 168.2 (Apr. 1968).

[63] A. Glezer Moshe, E. Farber, and G. Deutscher. "Granular superconductors for high kinetic inductance and low loss quantum devices". In: *Applied Physics Letters* 117.6 (Aug. 2020).

[64] R. W. Boyd. *Nonlinear optics.* San Diego, CA: AcadPr, 1992.

[65]   R. Vijay, D. H. Slichter, and I. Siddiqi. "Observation of Quantum Jumps in a Superconducting Artificial Atom". In: *Physical Review Letters* 106.11 (Mar. 2011).

[66]   A. B. Zorin. "Josephson Traveling-Wave Parametric Amplifier with Three-Wave Mixing". In: *Physical Review Applied* 6.3 (Sept. 2016).

[67]   R. Landauer. "Shock Waves in Nonlinear Transmission Lines and Their Effect on Parametric Amplification". In: *IBM Journal of Research and Development* 4.4 (Oct. 1960).

[68]   M. J. Madou. *Fundamentals of microfabrication and nanotechnology: 2 : Manufacturing techniques for microfabrication and nanotechnology*. Boca Raton, FL: CRC, 2012.

[69]   J. Hinze and K. Ellmer. "In situ measurement of mechanical stress in polycrystalline zinc-oxide thin films prepared by magnetron sputtering". In: *Journal of Applied Physics* 88.5 (Sept. 2000).

[70]   G. J. Dolan. "Offset masks for lift-off photoprocessing". In: *Applied Physics Letters* 31.5 (Sept. 1977).

[71]   N. Parekh and J. Price. "Cl Level Effects on Corrosion for Various Metallization Systems". In: *Journal of The Electrochemical Society* 137.7 (July 1990).

[72]   S. Mayumi et al. "Post-Treatments for Reactive Ion Etching of Al-Si-Cu Alloys". In: *Journal of The Electrochemical Society* 137.8 (Aug. 1990).

[73]   J. Verjauw et al. "Investigation of Microwave Loss Induced by Oxide Regrowth in High-Q Niobium Resonators". In: *Physical Review Applied* 16.1 (July 2021).

[74]   D. Niepce et al. "Geometric scaling of two-level-system loss in superconducting resonators". In: *Superconductor Science and Technology* 33.2 (Jan. 2020).

[75]   J. Burnett, L. Faoro, and T. Lindström. "Analysis of high quality superconducting resonators: consequences for TLS properties in amorphous oxides". In: *Superconductor Science and Technology* 29.4 (Mar. 2016).

[76]   H. Sundani. "Design and Fabrication of a Micro-Machined Free-Floating Membrane on a Flexible Substrate". Master's thesis. University of Toledo, 2010.

[77]   C.-Y. Lee, Y. Liu, and T. Itoh. "The effects of the coupled slotline mode and air-bridges on CPW and NLC waveguide discontinuities". In: *IEEE Transactions on Microwave Theory and Techniques* 43.12 (Dec. 1995).

[78]   M. Abuwasib, P. Krantz, and P. Delsing. "Fabrication of large dimension aluminum air-bridges for superconducting quantum circuits". In: *Journal of Vacuum Science & Technology B Microelectronics and Nanometer Structures* 31 (Apr. 2013).

[79]   Z.-C. Jin et al. "Fabrication of Al air-bridge on coplanar waveguide". In: *Chinese Physics B* 27.10 (Oct. 2018).

[80]   V. Papageorgiou, A. Khalid, and D. R. S. Cumming. "One-step air bridge fabrication technique using 3D e-beam lithography". In: *Proceedings of the 39th International Conference on Micro and Nano Engineering*. London, UK, Sept. 2013.

[81]   D. P. Pappas et al. "Two Level System Loss in Superconducting Microwave Resonators". In: *IEEE Transactions on Applied Superconductivity* 21.3 (June 2011).

[82]   N. Court, A. Ferguson, and R. Clark. "Energy gap measurement of nanostructured aluminium thin films for single Cooper-pair devices". In: *Superconductor Science and Technology* 21 (June 2007).

[83]   C. Schneider. "Magnetic Coupling between Superconducting Circuits and a Cantilever". PhD thesis. University of Innsbruck, May 2021.

Appendix A

Fabrication Recipe

Alignment Layer	
wafer cleaning	5 min in Acetone and 3 min in isopropanol + ultrasonication
resist spinning	MMA at 4000 rpm for 100 s
baking	5 min on 200 °C hot plate
resist spinning	PMMA at 2000 rpm for 100 s
baking	5 min on 200 °C hot plate
e-beam lithography	dose: $300\,\mu C/cm^2$, acceleration voltage: 30 kV, structure: pre-alignment crosses
development	105 s in IPA/H_2O 3:1
rinse and dry	rinse in H_2O and blow dry with N_2
descum and gettering	2 min Ar + O_2 descum, 2 min Ti gettering
niobium evaporation	5 nm Ti deposition + 100 nm Nb deposition at 0.5 nm/s
lift off	5 min in NMP at 70 °C + 3 min in IPA at 70 °C with ultrasonication
rinse and dry	rinse in IPA and blow dry with N_2
resist spinning	MMA at 4000 rpm for 100 s
baking	5 min on 200 °C hot plate
resist spinning	PMMA at 2000 rpm for 100 s
baking	5 min on 200 °C hot plate
e-beam lithography	dose: $300\,\mu C/cm^2$, acceleration voltage: 30 kV structure: alignment layer
development	105 s in IPA/H_2O 3:1
rinse and dry	rinse in H_2O and blow dry with N_2
descum and gettering	2 min Ar + O_2 descum, 2 min Ti gettering
niobium evaporation	5 nm Ti deposition + 100 nm Nb deposition at 0.5 nm/s
lift off	5 min in NMP at 70 °C + 3 min in IPA at 70 °C with ultrasonication
rinse and dry	rinse in IPA and blow dry with N_2

Table A.1: Vacuum-gap microstrip fabrication process. Part 1

Base Layer	
resist spinning	MMA at 4000 rpm for 100 s
baking	5 min on 200 °C hot plate
resist spinning	PMMA at 2000 rpm for 100 s
baking	5 min on 200 °C hot plate
e-beam lithography	dose: $800\,\mu C/cm^2$ for 150 nm lines $300\,\mu C/cm^2$ for the rest, acceleration voltage: 30 kV, structure: base layer
development	105 s in IPA/H_2O 3:1
rinse and dry	rinse in H_2O and blow dry with N_2
descum and gettering	2 min Ar + O_2 descum, 2 min Ti gettering
niobium evaporation	5 nm Ti deposition + 100 nm Nb deposition at 0.5 nm/s
lift off	5 min in NMP at 70 °C + 3 min in IPA at 70 °C with ultrasonication
rinse and dry	rinse in IPA and blow dry with N_2
Sacrificial Resist Layer	
cleaning	10 min O_2 plasma cleaning
resist spinning	MaN 2401 from *micro resist technology* at 4000 rpm for 30 s
baking	1 min on 90 °C hot plate
e-beam lithography	dose: $300\,\mu C/cm^2$, acceleration voltage: 30 kV structure: sacrificial resist layer
development	18 s in maD-377/H_2O 1:1
rinse and dry	rinse in H_2O and blow dry with N_2
Ground Plane Deposition	
argon milling	2 min, 400 V, 80 V, 20 mA, 10 sccm Ar milling
aluminum evaporation	10 nm Al evaporation at 0.1 nm/s and at 30° inclined planetary rotation
niobium sputtering	200 nm Nb sputter deposition at 0.175 nm/s, 3 mTorr, 400 V and 1 A
aluminum evaporation	50 nm Al evaporation at 0.1 nm/s

Table A.2: Vacuum-gap microstrip fabrication process. Part 2

Hole Mask Creation	
resist spinning	CSAR AR-P 6200.09 from *Allresist* at 2000 rpm for 100 s
baking	1 min on 150 °C hot plate
development	75 s in AR-P 600-546
rinse and dry	rinse in IPA and blow dry with N_2
chamber preparation	10 min O_2 plasma cleaning
aluminum etching	134 s BCl_3 Ar plasma etching until Nb layer is reached +15 s overetch
CF_4 conversion	30 s CF_4 plasma etching.
O_2 resist removal	50 s O_2 plasma etching until resist mask is removed +60 s overetch
Wafer Dicing	
resist spinning	PMMA at 2000 rpm for 100 s
baking	1 min on 100 °C hot plate
gluing to copper stencil	*Crystalbond^{TM} 555HMP*
laser dicing	first dicing contour
remove copper stencil	dissolve glue in hot distilled water bath
rinse and dry	rinse in H_2O and blow dry with N_2
glueing to copper stencil	*Crystalbond^{TM} 555HMP*
laser dicing	second dicing contour
remove copper stencil	dissolve glue in hot distilled water bath and remove individual chips
rinse and dry	rinse individual chips in H_2O and blow dry with N_2
Hole Etching and Sacrificial Resist Removal	
chamber preparation	10 min O_2 plasma cleaning
niobium etching	145 s CF_4 plasma etching until Al layer is reached +15 s overetch
niobium overetch	20 s CF_4 plasma etching.
Ar milling	3×15 s Ar plasma milling until resist is reached +15 s overetch
sacrificial resist removal	6 h 10 Pa O_2 plasma etching

Table A.3: Vacuum-gap microstrip fabrication process. Part 3